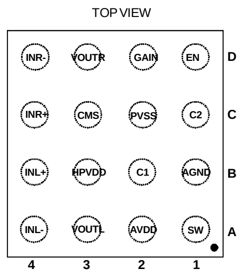
A22H165

High-performance class-G stereo headphone amplifier

Datasheet - production data

A22H165 - Flip-chip

Pinout (top view)



Balls are underneath

Features

- Power supply range: 2.3 V to 4.8 V
- 0.6 mA/channel quiescent current
- 2.1 mA current consumption with 100 µW/channel (10 dB crest factor)
- 0.006% typical THD+N at 1 kHz
- 100 dB typical PSRR at 217 Hz
- 100 dB of SNR A-weighted at G = 0 dB
- Zero "pop and click"
- Gain settings: 0 dB and 6 dB
- Integrated high efficiency step-down converter
- Low standby current: 5 µA max
- Output-coupling capacitors removed
- Thermal shutdown
- Flip-chip package: 1.65 mm x 1.65 mm, 400 µm pitch, 16 bumps

Applications

- Cellular / smart phones
- Portable media player
- Wearable
- Fitness and healthcare

Description

The A22H165 is a class-G stereo headphone driver dedicated to high-performance audio, high power efficiency and space-constrained applications. It is based on the core technology of a low power dissipation amplifier combined with a high efficiency step-down DC-DC converter for supplying this amplifier. When powered by a battery, the internal step down DC-DC converter generates the appropriate voltage to the amplifier depending on the amplitude of the audio signal to supply the headsets. It achieves a total 2.1 mA current consumption at 100 µW output power (10 dB crest factor). THD+N is 0.02 % maximum at 1 kHz and PSRR is 100 dB at 217 Hz, which ensures a high audio quality of the device in a wide range of environments. The traditionally bulky output coupling capacitors can be removed. A dedicated common-mode sense pin removes parasitic ground noise. The A22H165 is designed to be used with an output serial resistor. It ensures unconditional stability over a wide range of capacitive loads. The A22H165 is packaged in a tiny 16-bump flip-chip package with a pitch of 400 µm.

Table 1. Device summary

Order code	Temperature range	Package	Packing	Marking
A22H165	-40°C to +85°C	Flip-chip	Tape & reel	21

This is information on a product in full production. www.st.com

Contents

1 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1] during 1 ms.	5.5	V
V_{in+},V_{in-}	Input voltage referred to ground	+/- 1.2	V
Control input voltage	EN, Gain	-0.3 to VDD	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature[2]	150	°C
R_{thja}	Thermal resistance junction to ambient [3]	200	°C/W
P_d	Power dissipation	Internally limited[4]	
ESD	Human body model (HBM)[5] All pins VOUTR, VOUTL vs. AGND	 2 4	kV
	Machine model (MM), min. value[6]	100	V
	Charge device model (CDM) All pins VOUTR, VOUTL	 500 750	V
	IEC61000-4-2 level 4, contact[7] IEC61000-4-2 level 4, air discharge[7]	+/- 8 +/- 15	kV
	Lead temperature (soldering, 10 sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. Thermal shutdown is activated when maximum junction temperature is reached.
3. The device is protected from over temperature by a thermal shutdown mechanism, active at 150° C.
4. Exceeding the power derating curves for long periods may provoke abnormal operation.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. The measurement is performed on an evaluation board, with ESD protection EMIF02-AV01F3.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.3 to 4.8	V
HPVDD	internal step-down DC output voltages High rail voltage Low rail voltage	 1.9 1.2	V
EN,GAIN	Input voltage low level	0.6 V max	V
EN,GAIN	Input voltage high level	1.3 V min	
R_L	Load resistor	≥ 16	Ω
C_L	Load capacitor Serial resistor of 12 Ω minimum, $R_L \geq 16$ Ω	0.8 to 100	nF
T_{oper}	Operating free air temperature range	-40 to +85	°C
R_{thja}	Flip-chip thermal resistance junction to ambient	90	°C/W

2 Typical application schematic

Figure 1. Typical application schematic for the A22H165

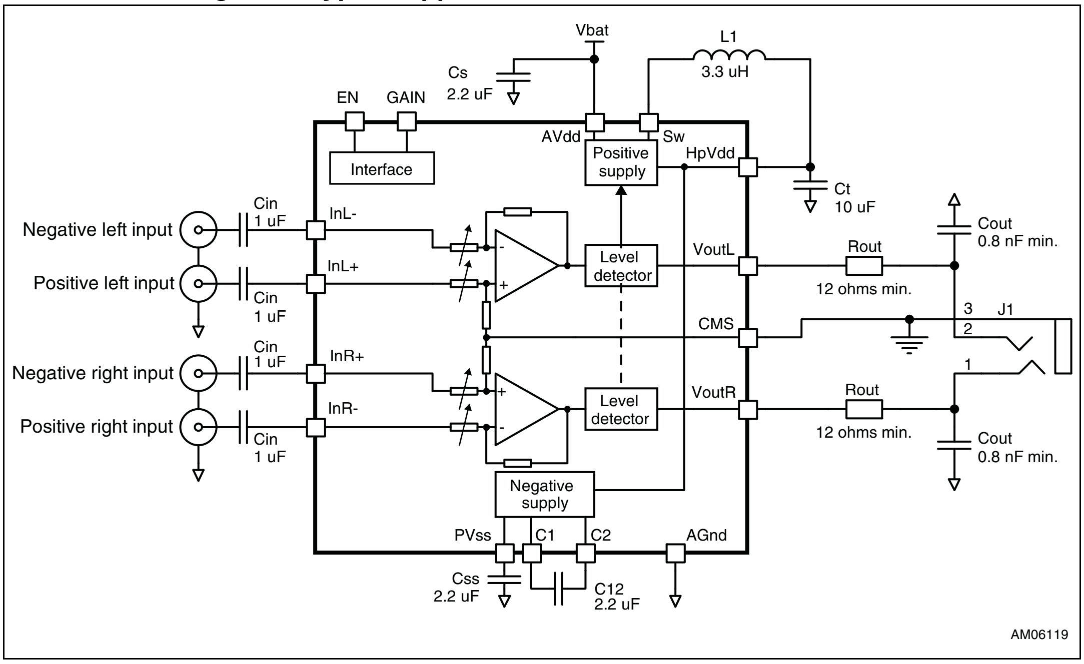


Table 4. A22H165 pin description

Pin n°	Pin name	Pin definition
A1	SW	Switching node of the buck converter
A2	AVDD	Analog supply voltage, connect to battery
A3	VOUTL	Output signal for left audio channel
A4	INL-	Negative input signal for left audio channel
B1	AGND	Device ground
B2	C1	Flying capacitor terminal for internal negative supply generator
B3	HPVDD	Buck converter output, power supply for amplifier
B4	INL+	Positive input signal for left audio channel
C1	C2	Flying capacitor terminal for internal negative supply generator
C2	PVSS	Negative supply generator output
C3	CMS	Common-mode sense, to be connected as close as possible to the ground of headphone/line out plug
C4	INR+	Positive input signal for right audio channel
D1	EN	Amplifier enable
D2	GAIN	Amplifier gain select
D3	VOUTR	Output signal for right audio channel
D4	INR-	Negative input signal for right audio channel

Table 5. A22H165 component description

Component[(1)]	Value	Description
Cs	2.2 µF	Decoupling capacitors for V_{CC}. A 2.2 µF capacitor is sufficient for proper decoupling of the A22H165. An X5R dielectric and 10 V rating voltage is recommended to minimize ΔC/ΔV when V_{CC} = 4.8 V. Must be placed as close as possible to the A22H165 to minimize parasitic inductance and resistance.
C12	2.2 µF	Capacitor for internal negative power supply operation. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V. Must be placed as close as possible to the A22H165 to minimize parasitic inductance and resistance.
C_{SS}	2.2 µF	Filtering capacitor for internal negative power supply. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V.
C_{in}	$Cin = \frac{1}{2 \times \pi \times Rin \times Fc}$	Input coupling capacitor that forms with $R_{in} \approx R_{indiff}/2$ a first-order high-pass filter with a -3 dB cut-off frequency Fc.
C_{out}	0.8 to 100 nF	Output capacitor of 0.8 nF minimum to 100 nF maximum. This capacitor is mandatory for operation of the A22H165.
R_{out}	12 Ω min.	Output resistor in-series with the A22H165 output. This 12 Ω minimum resistor is mandatory for operation of the A22H165.
L1	3.3 µH	Inductor for internal DC-DC step-down converter. References of inductors: refer to *Section 4.3.1* for more information.
C_t	10 µF	Tank capacitor for internal DC-DC step-down converter. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V. Refer to *Section 4.3.2* for more information.

1. Refer to *Section 4.3* for a complete description of each component.

3 Electrical characteristics

The values given in the following table are for the conditions V_{CC} = +3.6 V, AGND = 0 V, GAIN = 0 dB, R_L= 32 Ω + 15 Ω, T_{amb} = 25° C, unless otherwise specified.

Table 6. Electrical characteristics of the amplifier

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Quiescent supply current, no input signal, both channels enabled		1.2	1.5	mA
I_s	Supply current, with input modulation, both channels enabled, HPVDD = 1.2 V, output power per channel, F = 1 kHz Pout = 100 µW at 3 dB crest factor Pout = 500 µW at 3 dB crest factor Pout = 1 mW at 3 dB crest factor Pout = 100 µW at 10 dB crest factor Pout = 500 µW at 10 dB crest factor Pout = 1 mW at 10 dB crest factor		2.3 3.7 4.7 2.1 3.1 3.9	3.5 5 6.5	mA
I_{STBY}	Standby current, no input signal, V_{EN} = 0 V, V_{GAIN}=0V		0.6	5	µA
V_{in}	Input differential voltage range(1)			1	V_{rms}
V_{oo}	Output offset voltage No input signal	-500		+500	µV
V_{out}	Maximum output voltage, in-phase signals R_L = 16 Ω, THD+N = 1% max, f = 1 kHz R_L = 47 Ω, THD+N = 1% max, f = 1 kHz R_L = 10 kΩ, P_S = 15 Ω, C_L = 1 nF, THD+N = 1% max, f = 1 kHz	0.6 1.0 1.0	0.8 1.1 1.3		V_{rms}
THD+N	Total harmonic distortion + noise, G = 0 dB V_{out} = 700 mVrms, F = 1 kHz V_{out} = 700 mVrms, 20 Hz < F < 20 kHz		0.006 0.05	0.02	%
PSRR	Power supply rejection ratio(1), V_{ripple} = 200 mV_{pp}, grounded inputs F = 217 Hz, G = 0 dB, R_L ≥16 Ω F = 10 kHz, G = 0 dB, R_L ≥16 Ω	90	100 70		dB
CMRR	Common mode rejection ratio F = 1 kHz, G = 0 dB, V_{ic} = 200 mV_{pp} F = 20 Hz to 20 kHz, G = 0 dB, V_{ic} = 200 mV_{pp}		65 45		dB
Crosstalk	Channel separation R_L = 32 Ω + 15 Ω , G = 0 dB, F = 1 kHz, P_o = 10 mW	60	100		dB
SNR	Signal-to-noise ratio, A-weighted, V_{out} = 1 V_{rms}, THD+N < 1%, F = 1 kHz(1) G = +0 dB	100			dB
ONoise	Output noise voltage, A-weighted (1) G = +0 dB			9	µVrms

Table 6. Electrical characteristics of the amplifier (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
AV	Closed loop voltage gain, GAIN=L		0		dB
	Closed loop voltage gain, GAIN=H		6		dB
DAV	Gain matching between left and right channels	-0.5		+0.5	dB
R_{indiff}	Differential input impedance at 6 dB	24	33.2		kΩ
V_{IL}	Low level input voltage on EN, GAIN pins			0.6	V
V_{IH}	High level input voltage on EN, GAIN pins	1.3			V
I_{in}	Input current on EN,GAIN			10	µA

1. Guaranteed by design and parameter correlation.

Figure 2. Current consumption vs. power supply voltage

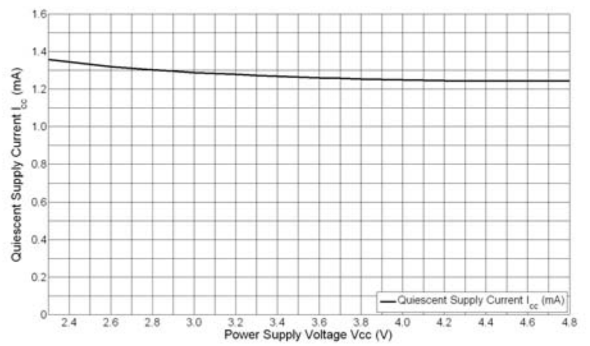


Figure 3. Standby current consumption vs. power supply voltage

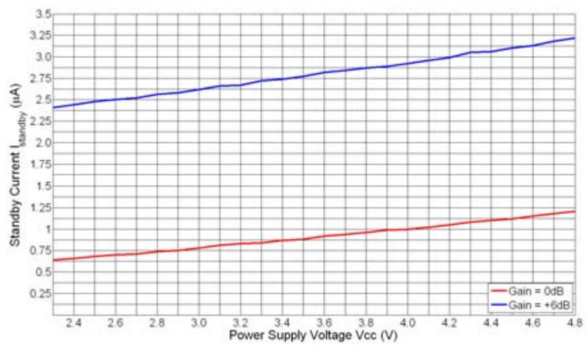


Figure 4. Maximum output power vs. power supply voltage, $R_L = 16\ \Omega$

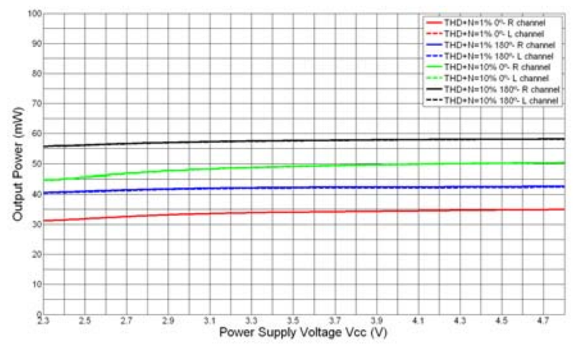


Figure 5. Maximum output power vs. power supply voltage, $R_L = 32\ \Omega$

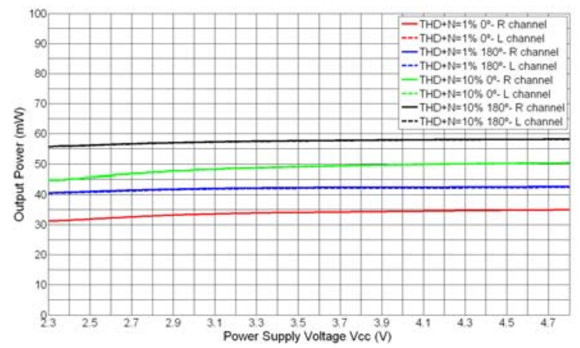


Figure 6. Maximum output power vs. power supply voltage, $R_L = 47\ \Omega$

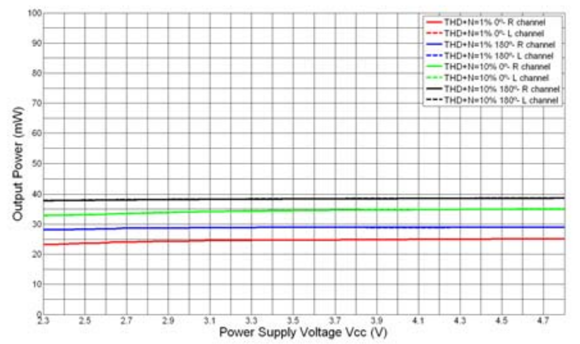


Figure 7. Current consumption vs. total output power, $R_L = 16\ \Omega$

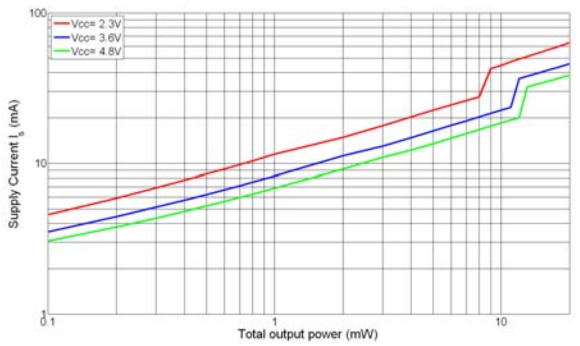


Figure 8. Current consumption vs. total output power, R_L = 32 Ω

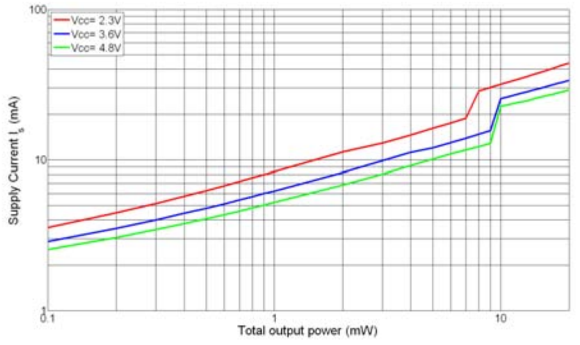


Figure 9. Current consumption vs. total output power, R_L = 47 Ω

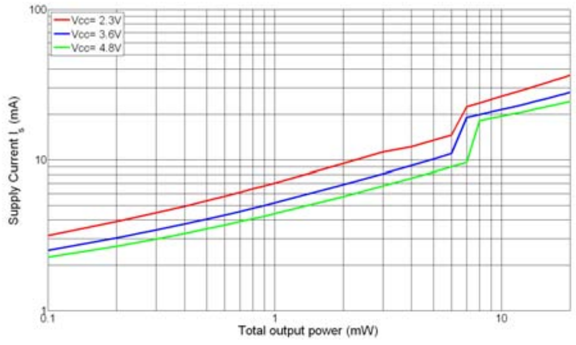


Figure 10. Differential input impedance vs. gain

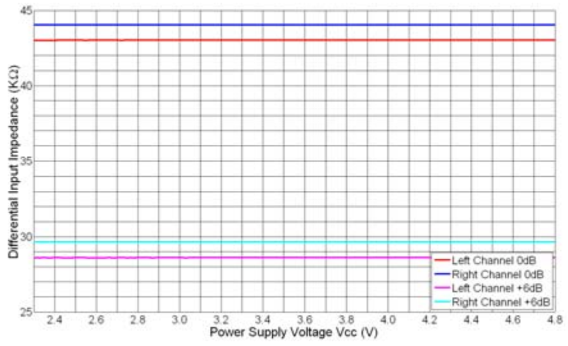


Figure 11. THD+N vs. output power - R_L = 16 Ω, in-phase, V_{CC} = 2.5 V

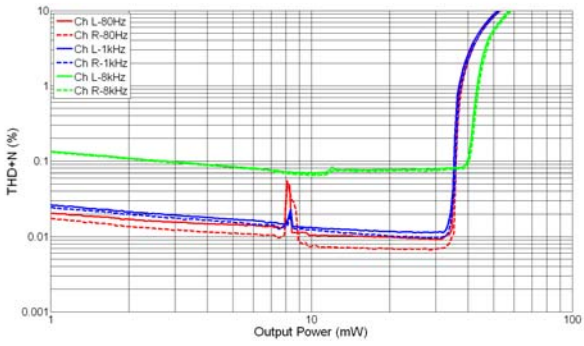


Figure 12. THD+N vs. output power - R_L = 16 Ω, out-of-phase, V_{CC} = 2.5 V

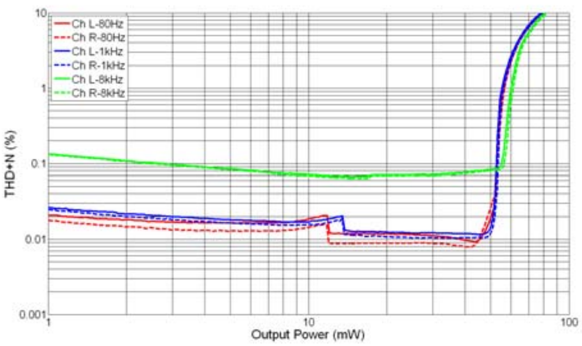


Figure 13. THD+N vs. output power - R_L = 16 Ω, in-phase, V_{CC} = 3.6 V

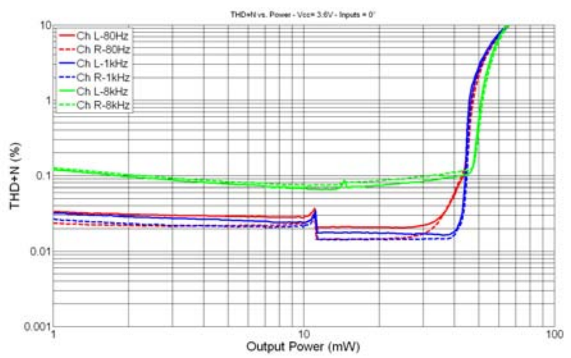


Figure 14. THD+N vs. output power - R_L = 16 Ω, out-of-phase, V_{CC} = 3.6 V

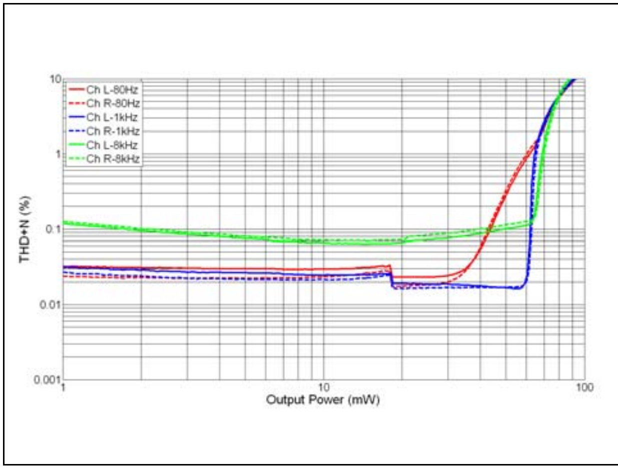


Figure 15. THD+N vs. output power - R_L = 16 Ω, in-phase, V_{CC} = 4.8 V

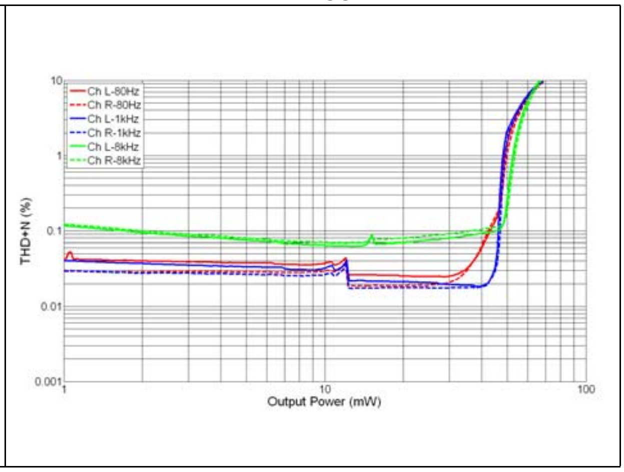


Figure 16. THD+N vs. output power - R_L = 16 Ω, out-of-phase, V_{CC} = 4.8 V

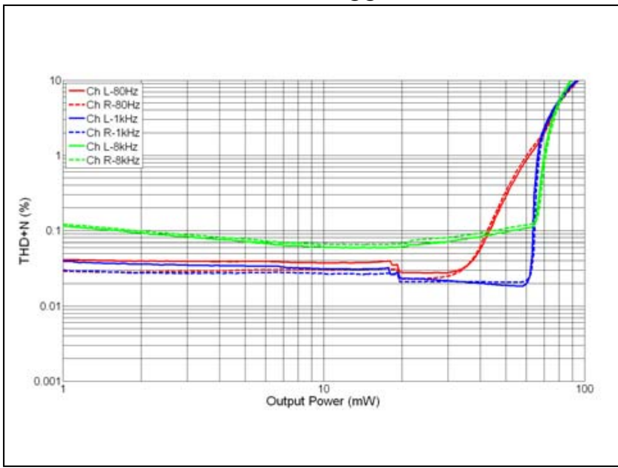


Figure 17. THD+N vs. output power - R_L = 32 Ω, in-phase, V_{CC} = 2.5 V

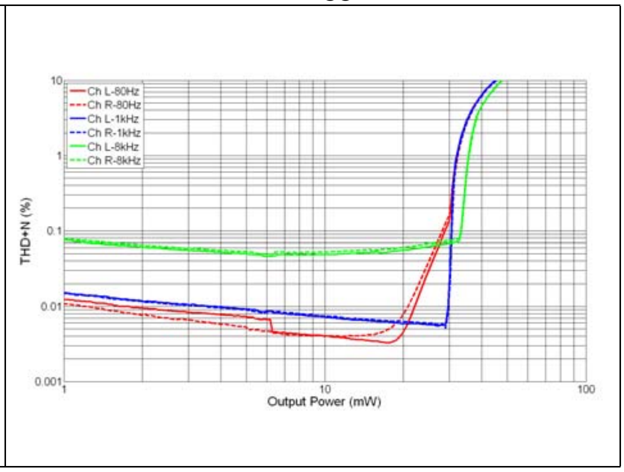


Figure 18. THD+N vs. output power - R_L = 32 Ω, out-of-phase, V_{CC} = 2.5 V

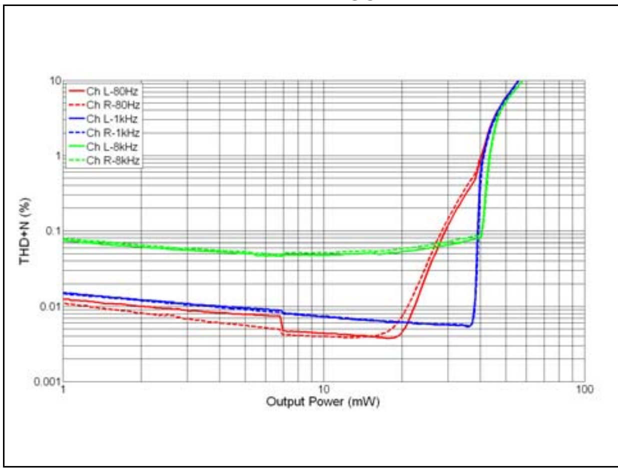


Figure 19. THD+N vs. output power - R_L = 32 Ω, in-phase, V_{CC} = 3.6 V

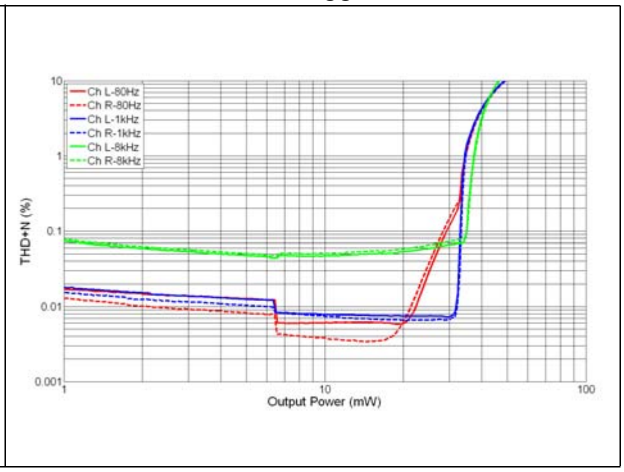


Figure 20. THD+N vs. output power - R_L = 32 Ω, out-of-phase, V_{CC} = 3.6 V

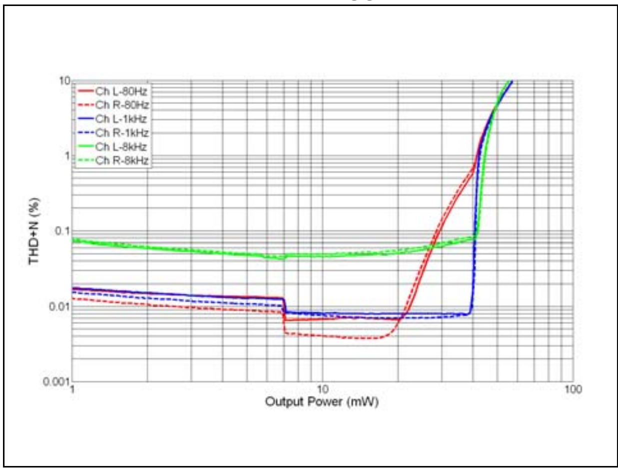


Figure 21. THD+N vs. output power - R_L = 32 Ω, in-phase, V_{CC} = 4.8 V

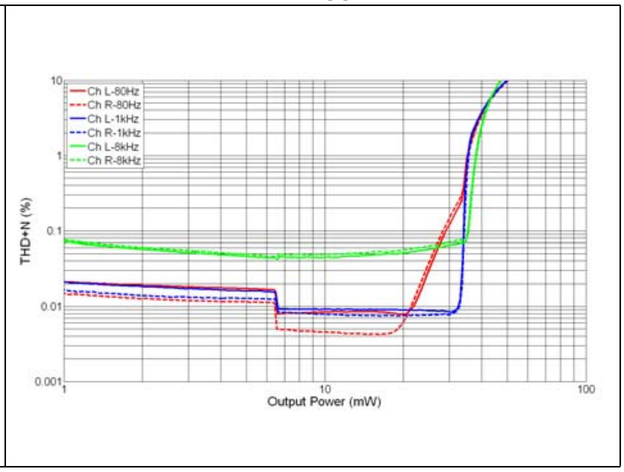


Figure 22. THD+N vs. output power - R_L = 32 Ω, out-of-phase, V_{CC} = 4.8 V

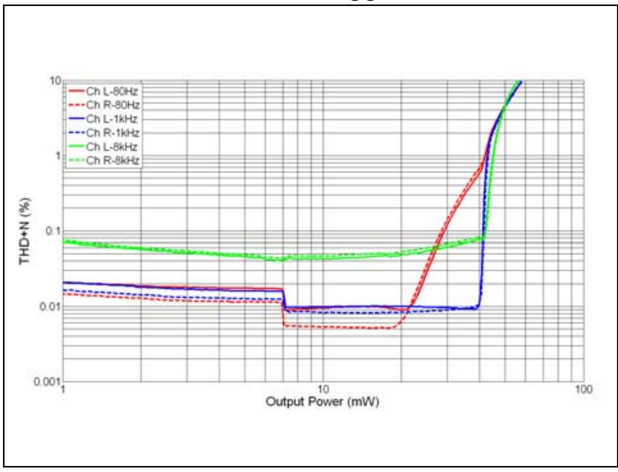


Figure 23. THD+N vs. output power - R_L = 32 Ω +IPad, in-phase, V_{CC} = 2.5 V

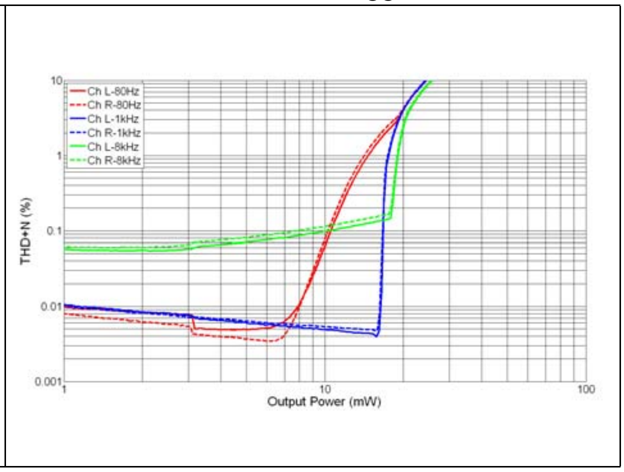


Figure 24. THD+N vs. output power - R_L = 32 Ω +IPad, out-of-phase, V_{CC} = 2.5 V

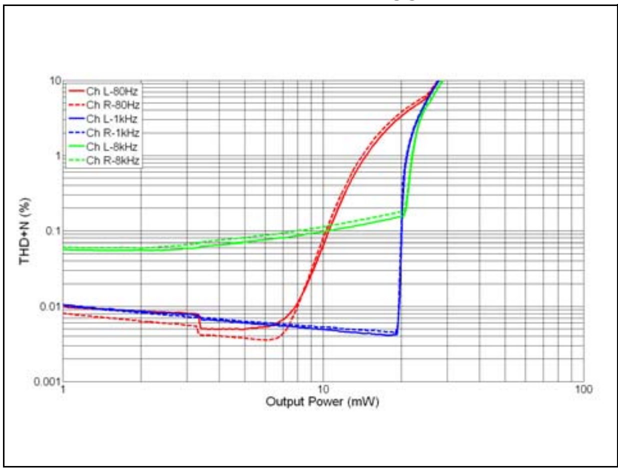


Figure 25. THD+N vs. output power - R_L = 32 Ω +IPad, in-phase, V_{CC} = 3.6 V

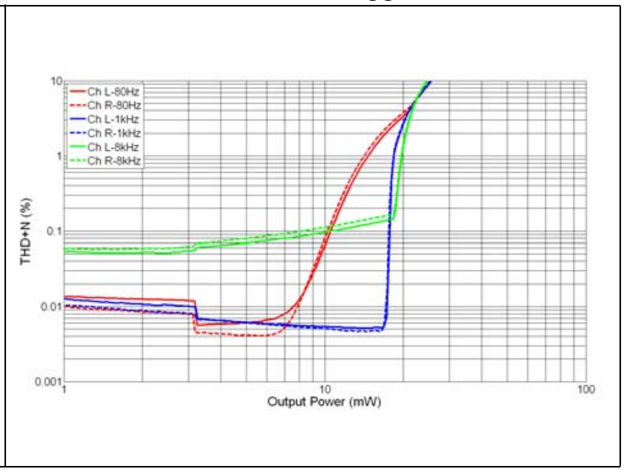


Figure 26. THD+N vs. output power - R_L = 32 Ω +IPad, out-of-phase, V_{CC} = 3.6 V

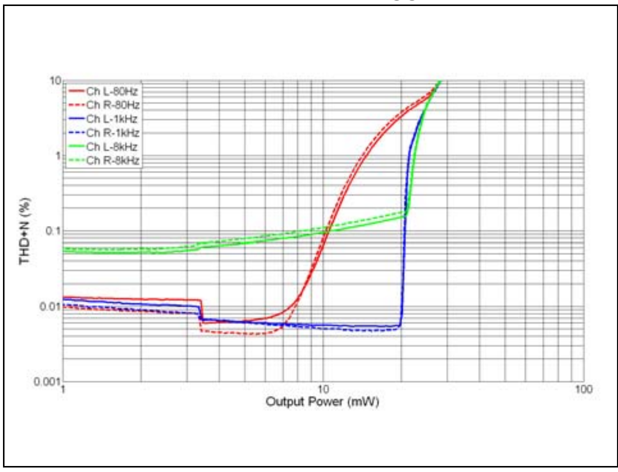


Figure 27. THD+N vs. output power - R_L = 32 Ω +IPad, in-phase, V_{CC} = 4.8 V

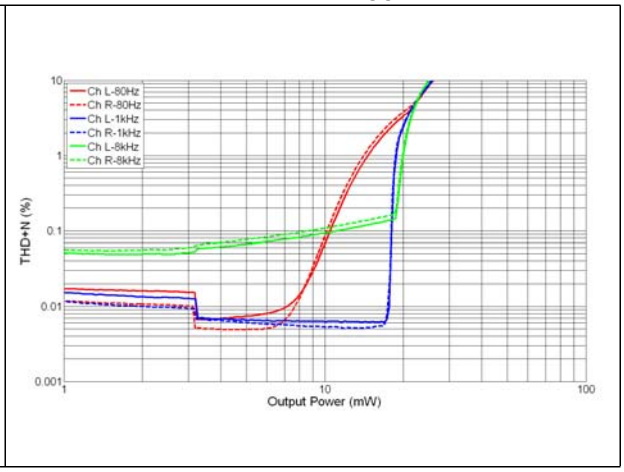


Figure 28. THD+N vs. output power - R_L = 32 Ω +IPad, out-of-phase, V_{CC} = 4.8 V

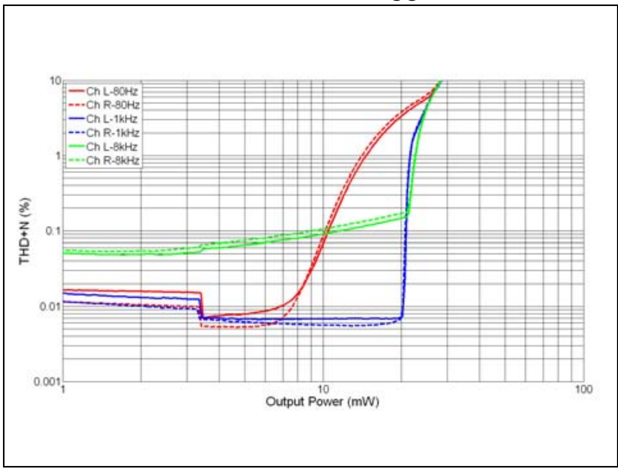


Figure 29. THD+N vs. output power - R_L = 47 Ω, in-phase, V_{CC} = 2.5 V

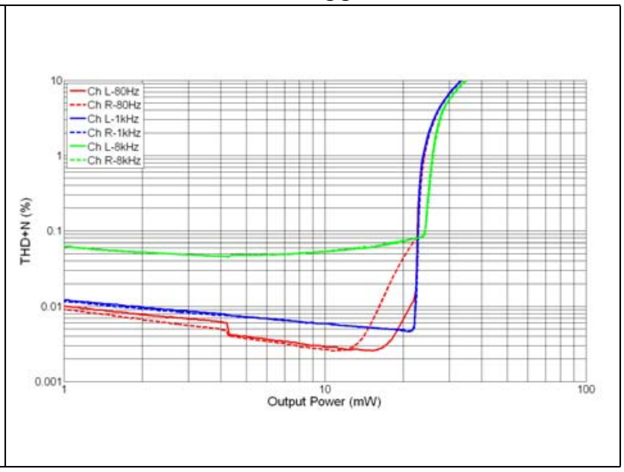


Figure 30. THD+N vs. output power - R_L = 47 Ω, out-of-phase, V_{CC} = 2.5 V

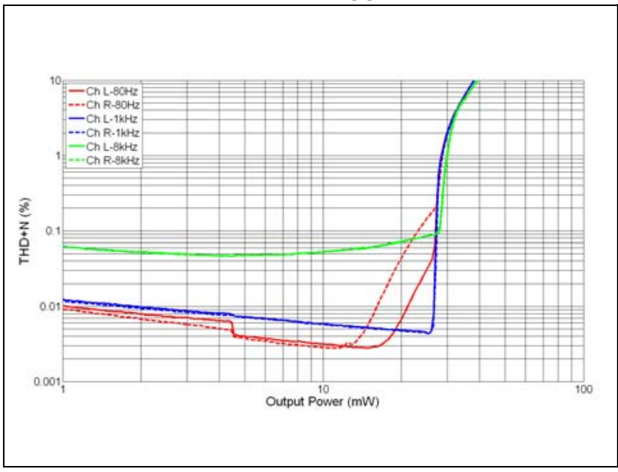


Figure 31. THD+N vs. output power - R_L = 47 Ω, in-phase, V_{CC} = 3.6 V

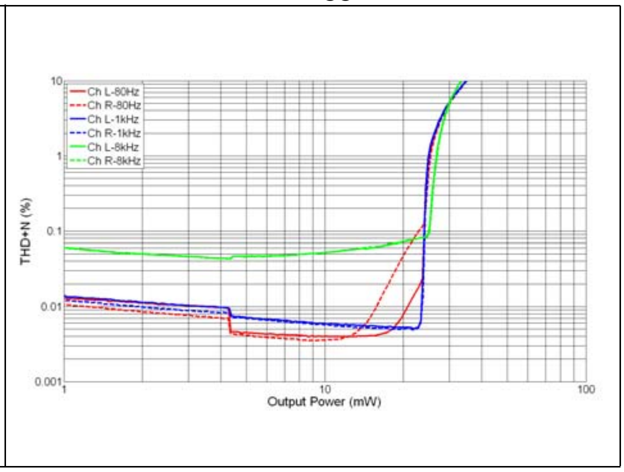


Figure 32. THD+N vs. output power - R_L = 47 Ω, out-of-phase, V_{CC} = 3.6 V

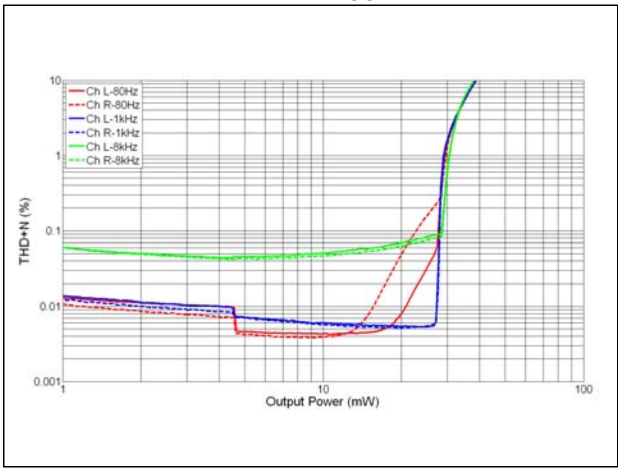


Figure 33. THD+N vs. output power - R_L = 47 Ω, in-phase, V_{CC} = 4.8 V

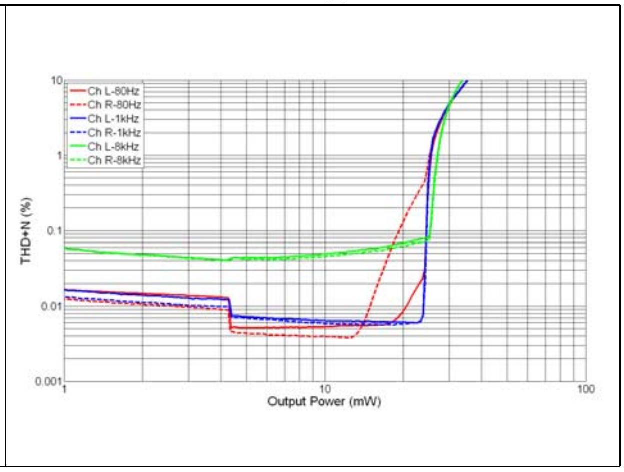


Figure 34. THD+N vs. output power - R_L = 47 Ω, out-of-phase, V_{CC} = 4.8 V

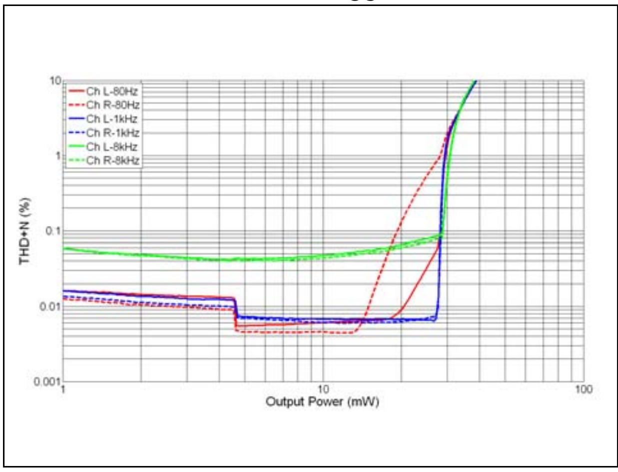


Figure 35. THD+N vs. frequency, R_L = 16 Ω, in-phase, V_{CC} = 2.5 V

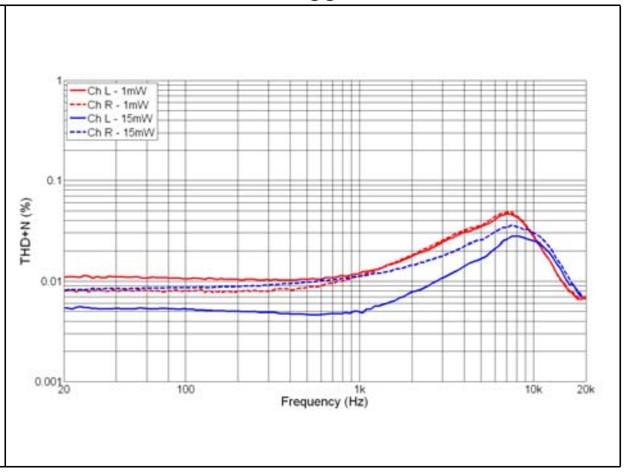


Figure 36. THD+N vs. frequency, R_L = 16 Ω, out-of-phase, V_{CC} = 2.5 V

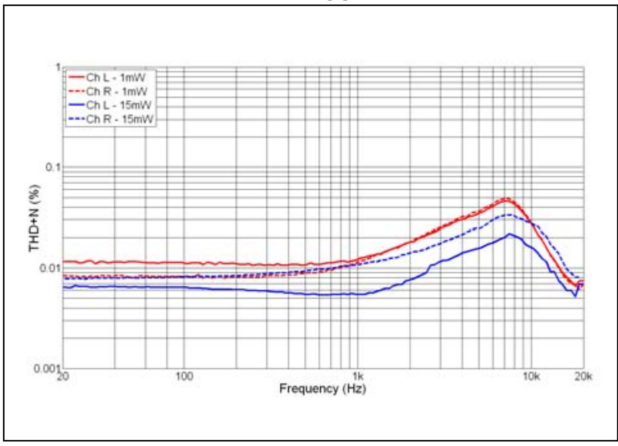


Figure 37. THD+N vs. frequency, R_L = 16 Ω, in-phase, V_{CC} = 3.6 V

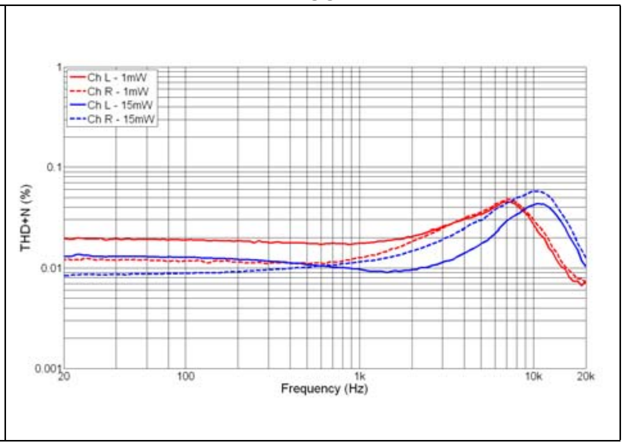


Figure 38. THD+N vs. frequency, R_L = 16 Ω, out-of-phase, V_{CC} = 3.6 V

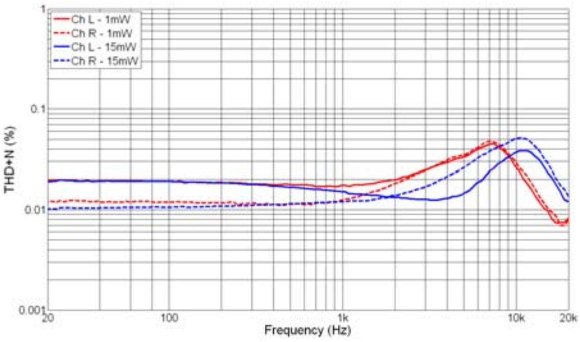


Figure 39. THD+N vs. frequency, R_L = 16 Ω, in-phase, V_{CC} = 4.8 V

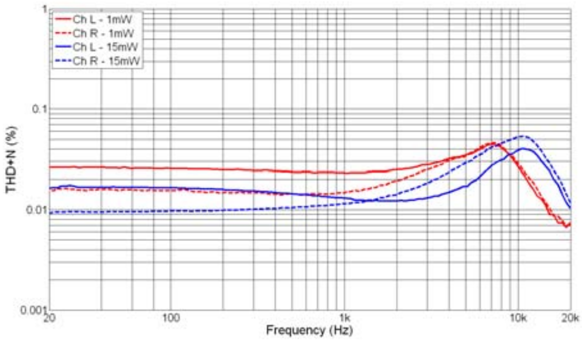


Figure 40. THD+N vs. frequency, R_L = 16 Ω, out-of-phase, V_{CC} = 4.8 V

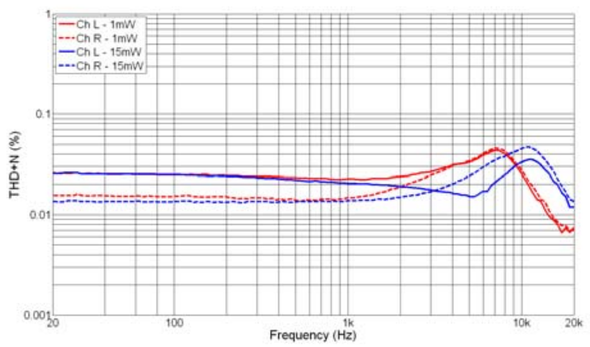


Figure 41. THD+N vs. frequency, R_L = 32 Ω, in-phase, V_{CC} = 2.5 V

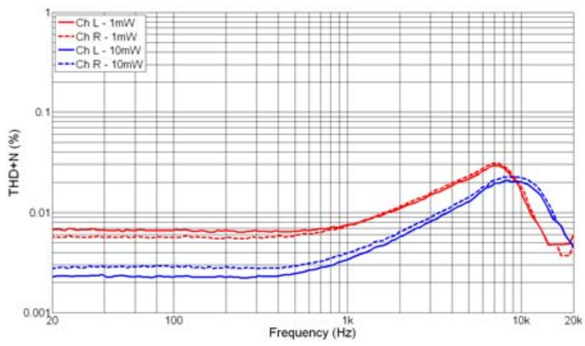


Figure 42. THD+N vs. frequency, R_L = 32 Ω, out-of-phase, V_{CC} = 2.5 V

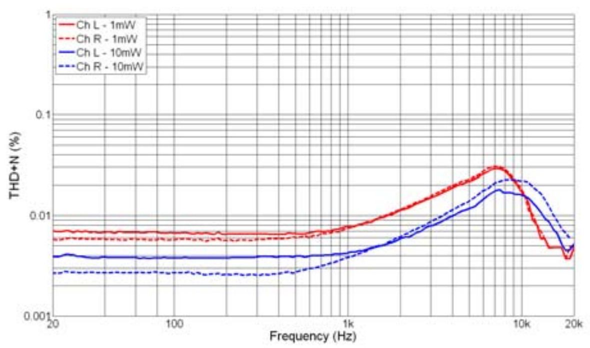


Figure 43. THD+N vs. frequency, R_L = 32 Ω, in-phase, V_{CC} = 3.6 V

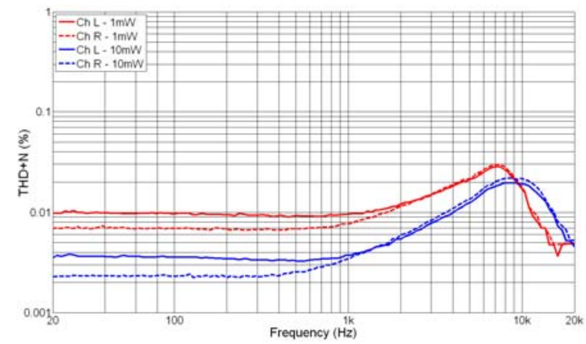


Figure 44. THD+N vs. frequency, R_L = 32 Ω, out-of-phase, V_{CC} = 3.6 V

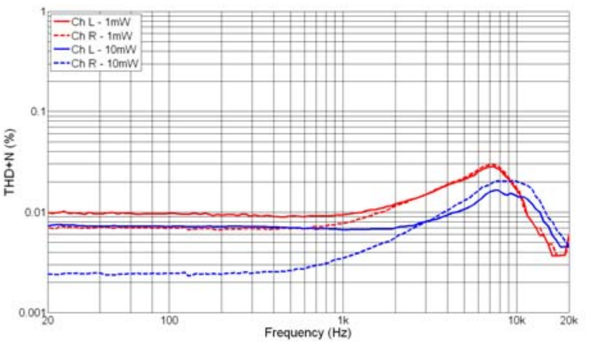


Figure 45. THD+N vs. frequency, R_L = 32 Ω, in-phase, V_{CC} = 4.8 V

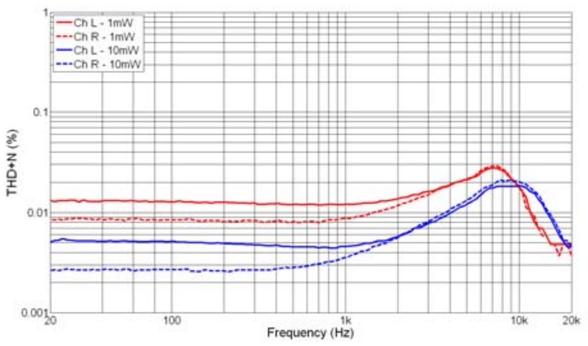


Figure 46. THD+N vs. frequency, R_L = 32 Ω, out-of-phase, V_{CC} = 4.8 V

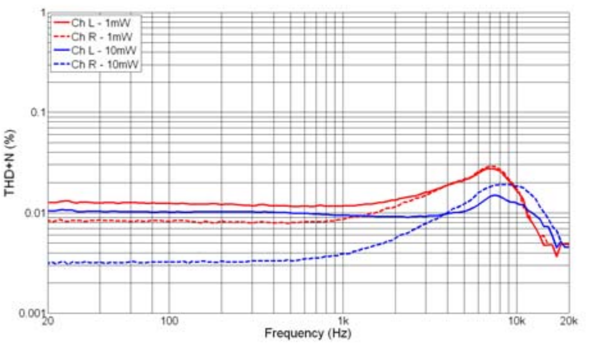


Figure 47. THD+N vs. frequency, R_L = 47 Ω, in-phase, V_{CC} = 2.5 V

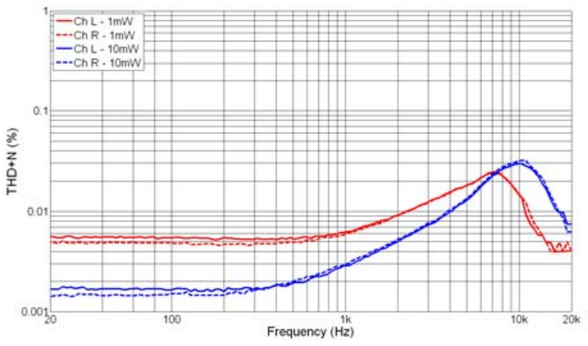


Figure 48. THD+N vs. frequency, R_L = 47 Ω, out-of-phase, V_{CC} = 2.5 V

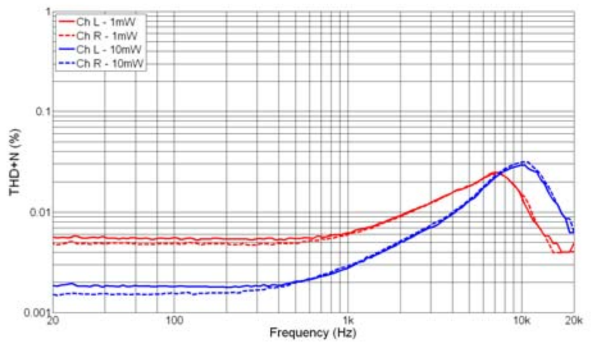


Figure 49. THD+N vs. frequency, R_L = 47 Ω, in-phase, V_{CC} = 3.6 V

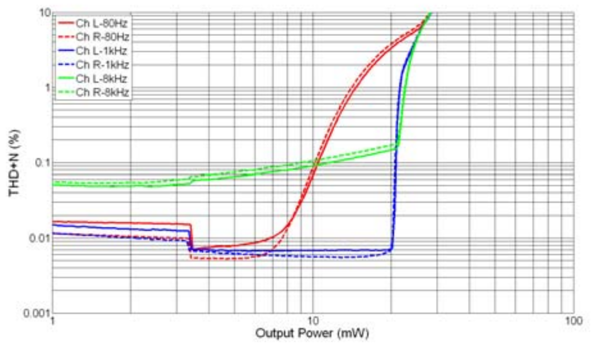


Figure 50. THD+N vs. frequency, R_L = 47 Ω, out-of-phase, V_{CC} = 3.6 V

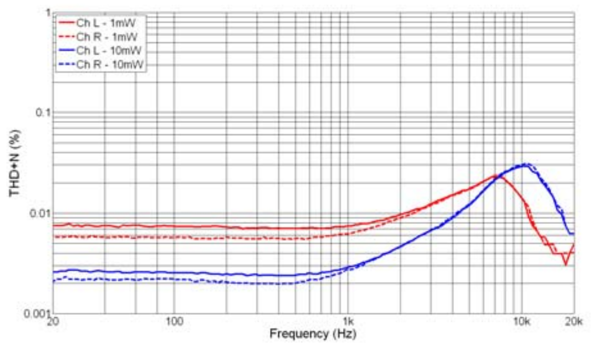


Figure 51. THD+N vs. frequency, R_L = 47 Ω, in-phase, V_{CC} = 4.8 V

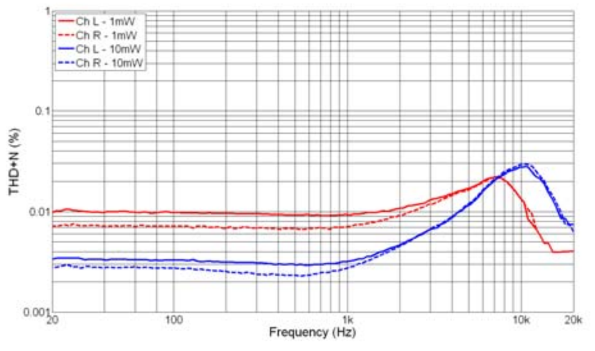


Figure 52. THD+N vs. frequency, R_L = 47 Ω, out-of-phase, V_{CC} = 4.8 V

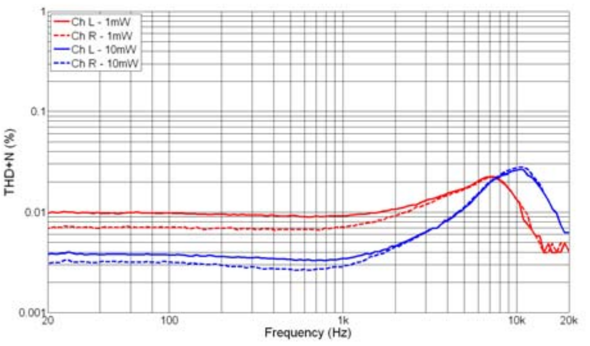


Figure 53. PSRR vs. frequency - V_{CC} = 3.6 V, gain = 0 dB

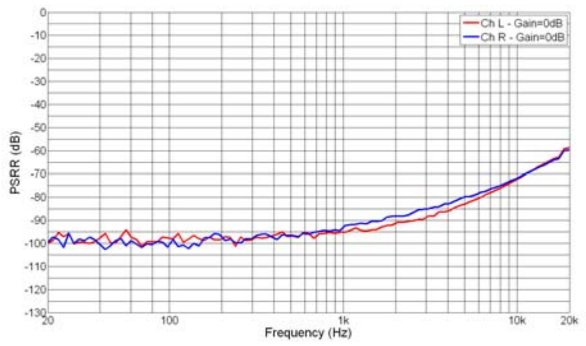


Figure 54. PSRR vs. frequency - V_{CC} = 3.6 V, gain = +6 dB

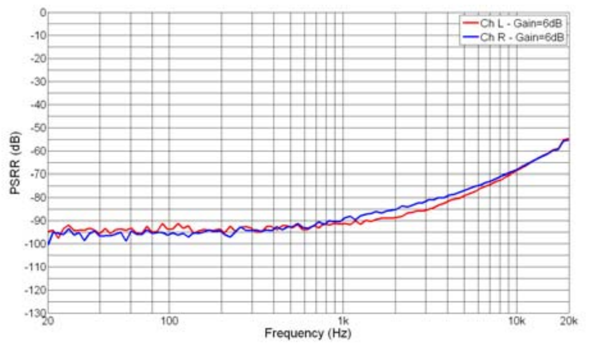


Figure 55. Output signal spectrum (V_{CC} = 3.6 V, load = 32 Ω)

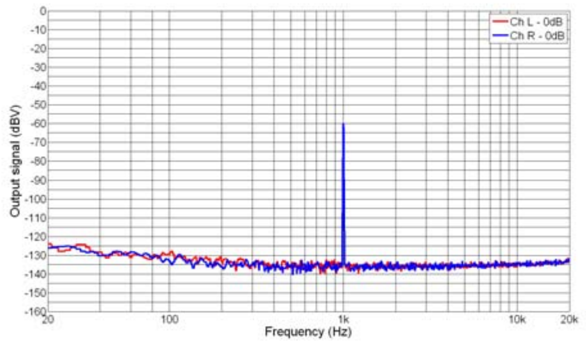


Figure 56. Crosstalk vs. frequency - R_L = 32 Ω, V_{CC} = 3.6 V, gain = 0 dB

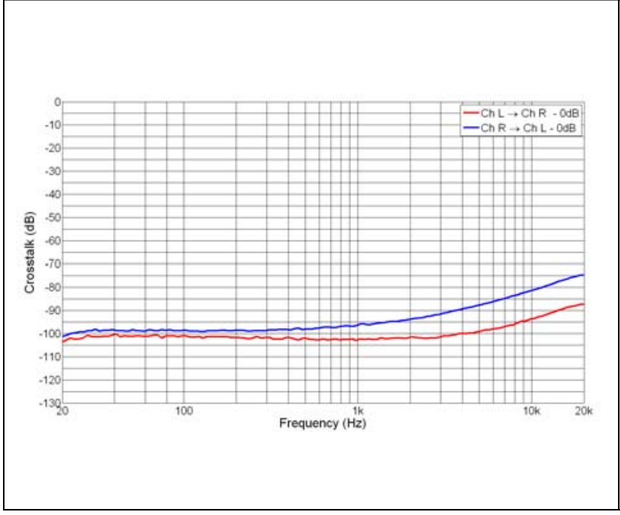


Figure 57. Crosstalk vs. frequency - R_L = 32 Ω, V_{CC} = 3.6 V, gain = +6 dB

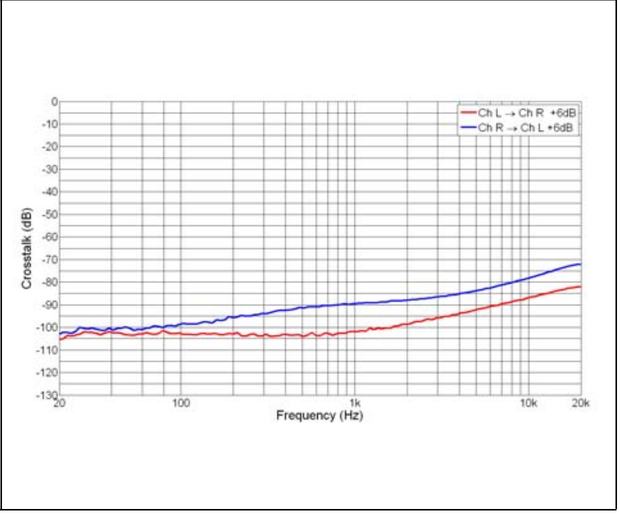


Figure 58. Crosstalk vs. frequency - R_L = 47 Ω, V_{CC} = 3.6 V, gain = 0 dB

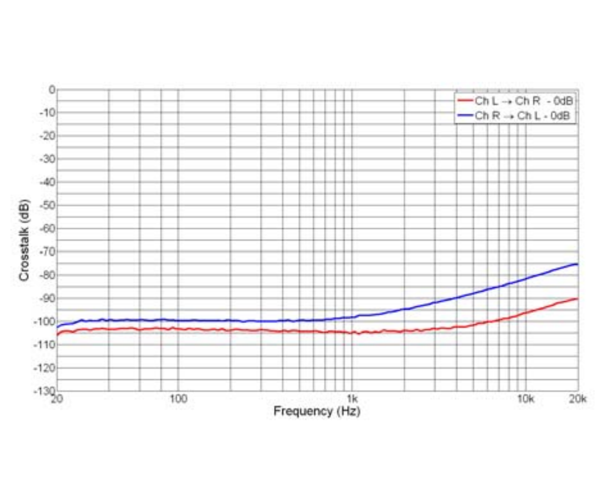


Figure 59. Crosstalk vs. frequency - R_L = 47 Ω, V_{CC} = 3.6 V, gain = +6 dB

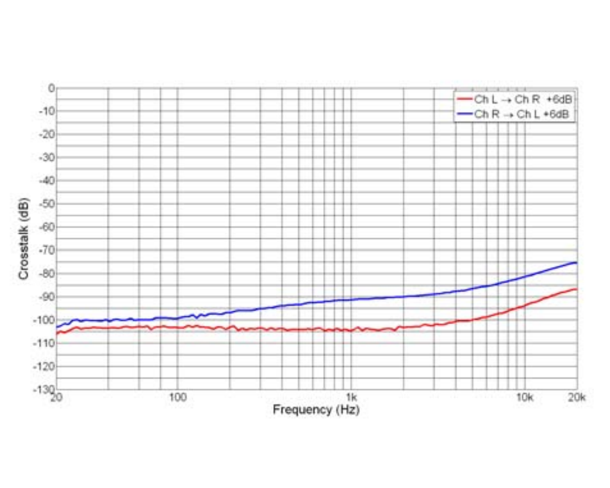


Figure 60. CMRR vs. frequency, 32 Ω, V_{CC} = 36 V, 0 dB

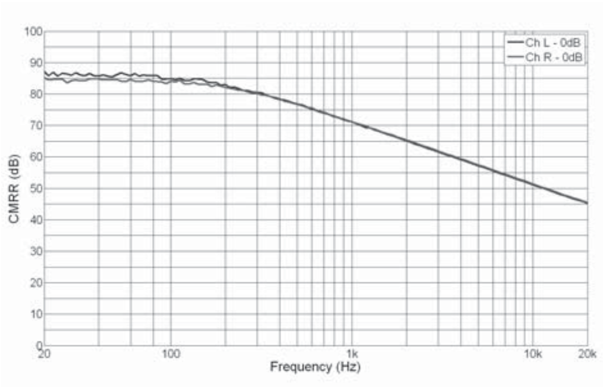


Figure 61. CMRR vs. frequency, 32 Ω, V_{CC} = 36 V, 6 dB

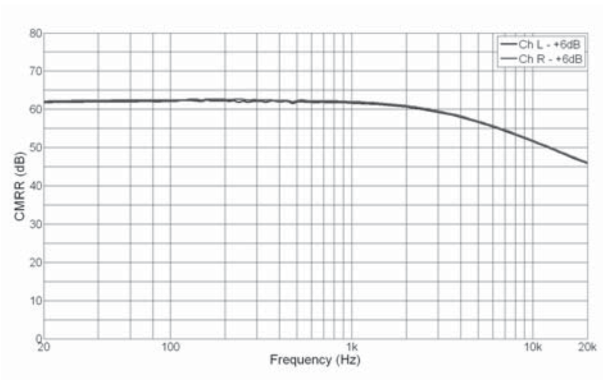


Figure 62. Wake-up time

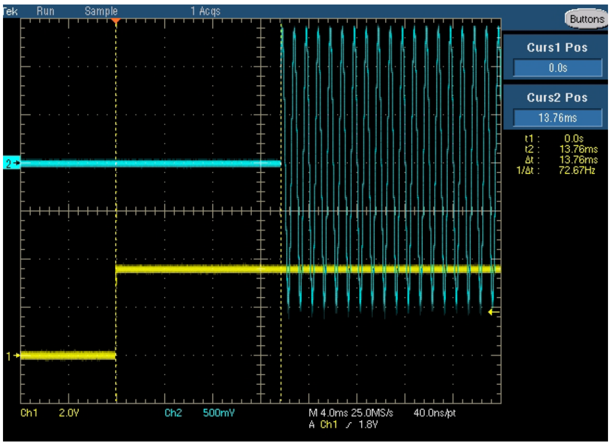
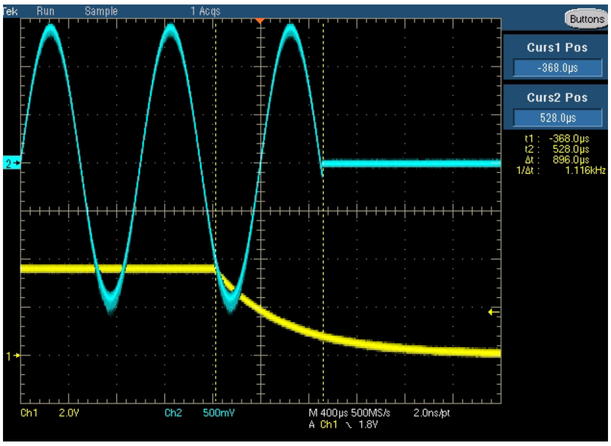


Figure 63. Shutdown



4 Application information

4.1 Gain control

The A22H165 has two gain settings which are controlled via the GAIN pin:

GAIN voltage	Amplifier gain
≤ 0.6 V	0 dB
≥ 1.3 V	6 dB

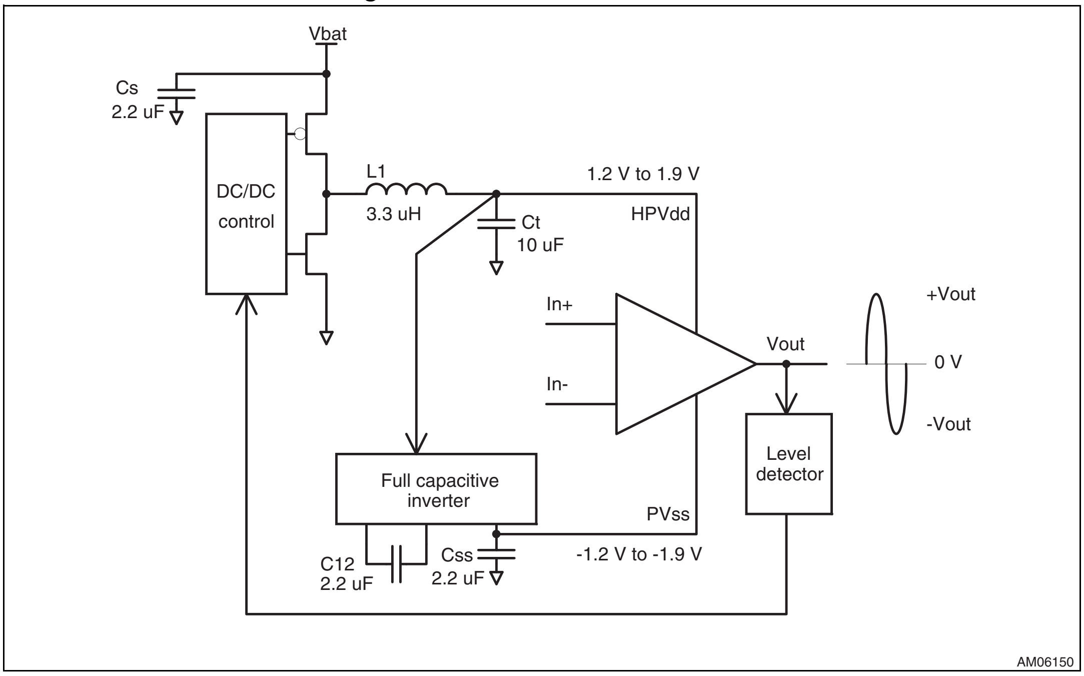
Note: See Table 6: Electrical characteristics of the amplifier for V_{IH} and V_{IL} levels.

4.2 Overview of the class-G, 2-level headphone amplifier

The A22H165 uses what is referred to as *class-G operating mode*. This mode is a combination of the class AB biasing technique and an adaptive power supply. For this device, the power supply uses two levels: ±1.2 V and ±1.9 V.

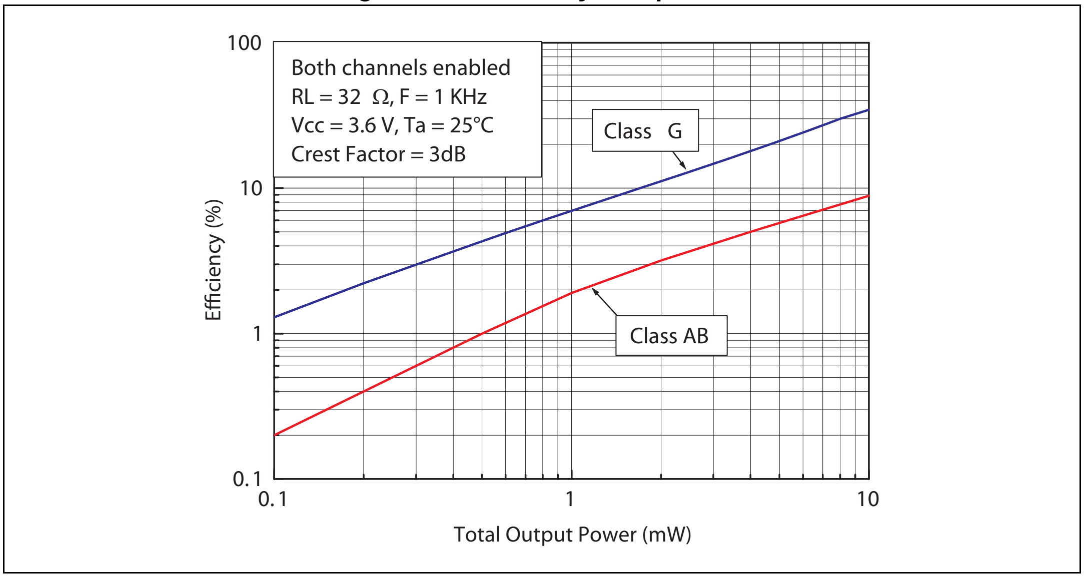
To create the ±1.2 V and ±1.9 V levels, the device uses an internal high-efficiency step-down converter linked with a fully capacitive inverter from AV_{dd}. Thanks to these internally-generated symmetrical power supply voltages, the output of the amplifier can be biased at 0 V, thus eliminating the classical bulky DC blocking output capacitors (typically more than 100 µF).

Figure 64. A22H165 architecture



When an audio signal is playing with the A22H165, the class G feature adjusts in real time the internal power supply voltage in order to achieve the best efficiency possible. In addition, thanks to the fast transient response of the internal DC-DC converters, the switching between ±1.2 V and ±1.9 V can be achieved without audio clipping. Moreover, the out-of-audio band DC-DC switching frequency keeps the audio quality at a high level (distortion, noise, etc…).

Figure 65. Efficiency comparison

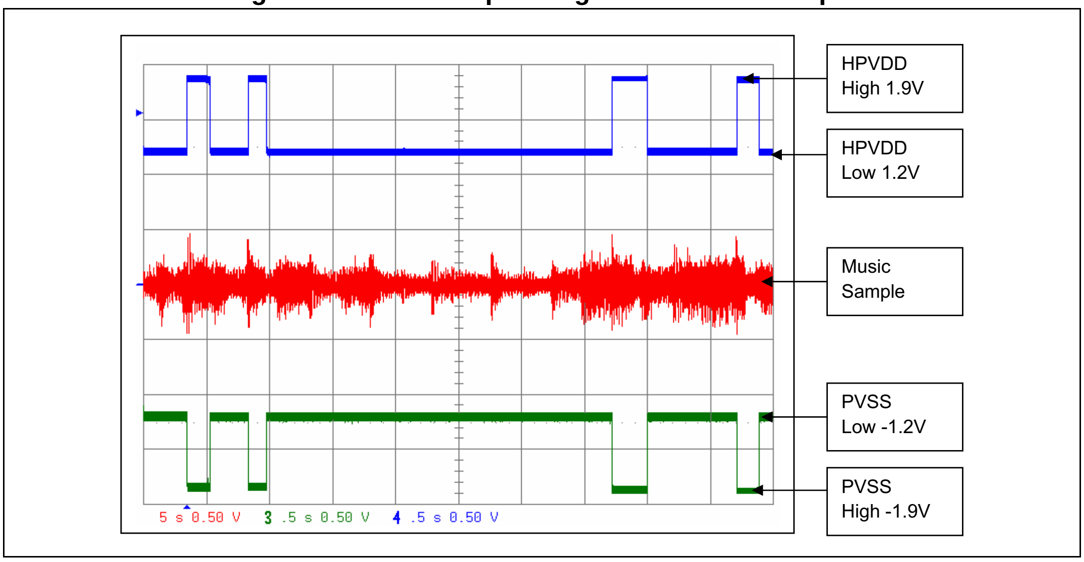


Most audio signals have a crest factor higher than 6 dB (10 dB on average), which means that most of the time the music level is low. In this case, the setting of the internal DC-DC converters is low (1.2 V) and in this way, helps to minimize the power dissipation.

When the audio signal amplitude increases due to a peak or louder music, the setting of the internal DC-DC converters increases to 1.9 V, automatically increasing the output dynamic range. This 1.9 V value remains until the end of the decay time.

Figure 66 shows a music sample played at high levels.

Figure 66. Class-G operating with a music sample



Note: *HPVDD/PVSS voltages are created internally by DC-DC converters. To avoid destruction of the A22H165 power amplifier, do not connect any external power supply on these pins.*

4.3 External component selection

The A22H165 requires few external passive components to operate correctly. Each component is described in the following sections.

4.3.1 Step-down inductor selection (L1)

The A22H165 needs one inductor for the internal step-down DC-DC converter. This inductor must fit the following constraints:

- Typical value: 2.2 µH to 3.3 µH (3.3 µH is recommended)
- Maximum current in operating mode: 400 mA
- Minimum inductor value at maximum current: 1.5 µH
- Maximum inductor value at zero current: 4.3 µH
- DC resistance: from 50 mΩ up to 450 mΩ

Table 7 shows the part number that should be used according to the inductor value.

Table 7. Recommended inductor

Manufacturer	Part number	Value
Murata	LQM21PN3R3NGRD	3.3 µH
	LQM2MPN3R3G0L	3.3 µH
	LQM2MPN2R2G0L	2.2 µH
FDK	MIPSZ2012D3R3	3.3 µH
	MIPSZ2012D2R2	2.2 µH

4.3.2 Step-down output capacitor selection (C_t)

For the internal DC-DC step-down converter, the A22H165 needs one output capacitor.

The three criteria for selecting the output capacitor are the range value of the capacitor including self tolerance, DC variation and the minimum ESR value, which is mandatory to avoid oscillation of the converter. Therefore the following constraints must be observed.

- Typical capacitor value: 10 µF at DC = 0 V
- Maximum capacitor value: 12 µF at DC = 0 V
- Minimum capacitor value: 4.8 µF at DC = 2 V
- Voltage range across this capacitor: from 1.1 V to 2 V
- Minimum DC ESR value: 5 mΩ

A ceramic capacitor in a 0603-type package is also recommended because of its close placement to the A22H165, which makes it easier to minimize parasitic inductance and resistance that have a negative impact on the audio performance.

Table 8. Recommended capacitors

Manufacturer	Part number	Value
Murata	GRM188R60J106ME47	10 µF, 6.3 V, X5R
	GRM188R60J106ME84	10 µF, 6.3 V, X5R
	GRM188R61E106ME73	10 µF, 25 V, X5R

4.3.3 Full capacitive inverter capacitors selection (C12 and C_{SS})

Two capacitors (C12 and C_{ss}) are needed for this internal DC-DC inverter.

The three criteria for selecting these capacitors are the range value of the capacitor including self tolerance, DC variation and the minimum ESR to minimize power losses.

- Typical capacitor value: 2.2 µF +/-20 %
- Voltage across these capacitors: from 1.1 V to 2 V
- Minimum capacitor value: 1 µF

Again, a ceramic capacitor in a 0603 or 0402-type package is also recommended because of their close placement to the A22H165, which makes it easier to minimize parasitic inductance and resistance that have a negative impact on the audio performance.

4.3.4 Power supply decoupling capacitor selection (Cs)

A 2.2 µF decoupling capacitor with low ESR is recommended for positive power supply decoupling. Packages such as the 0402 or 0603 are also recommended because of their close placement to the A22H165, which makes it easier to minimize parasitic inductance. It is advised to choose a X5R dielectric for capacitor tolerance, and a 10 V DC rating voltage for 4.8 V operations (or a 6.3 V DC rating voltage for 3.6 V operations), to take into consideration the ΔC/ΔV variation of this type of ceramic capacitor.

An important parameter is the rated voltage of the capacitor. A 2.2 µF/6.3 V capacitor used at 4.8 V DC typically loses about 40 % of its value. In fact, with a 4.8 V power supply voltage, the decoupling value is about 1.3 µF instead of 2.2 µF. Because the decoupling capacitor influences the THD+N in the medium-to-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots, which can be problematic if they reach the power supply's AMR value (5.5 V). This is why, for a 2.2 µF value, we recommend a 2.2 µF/10 V, a 4.7 µF/6.3 V or a ceramic capacitor with a low DC bias variation rated at 6.3 V.

4.3.5 Input coupling capacitor selection (C_{in})

C_{in} input coupling capacitors are mandatory for the A22H165's operation. They block any DC component coming from the audio signal source.

C_{in} with R_{in} form a first-order high-pass filter and the -3 dB cut-off frequency is:

$$FC(-3dB) = \frac{1}{2 \times \pi \times Rin \times Cin}$$

R_{in} is the single-ended input impedance that can be approximated at about $R_{indiff}/2$.

R_{in} also depends on the gain setting. *Figure 10* provides the differential input impedance vs. gain. One can also see that R_{indiff} is minimum for the maximum gain setting (that is, 6 dB). Therefore, in most cases, R_{in} should be set to 6 dB to calculate the minimum input capacitor C_{in}.

Example:

In this case and for a -3 dB cut-off frequency of 20 Hz, C_{in} = 0.64 µF. The closest normalized value is 0.68 µF but a 1 µF capacitor is more suitable to take into consideration the capacitor tolerance +/-20 %.

If the aim is to have the 20 Hz at -1 dB, the capacitor has to be multiplied by 1.96. As such, C_{in} = 0.64 x 1.96 = 1.25 µF. The closest normalized value would be 1.5 µF or 2.2 µF.

4.3.6 Low-pass output filter (R_{out} and C_{out}) and IEC 61000-4-2 ESD protection

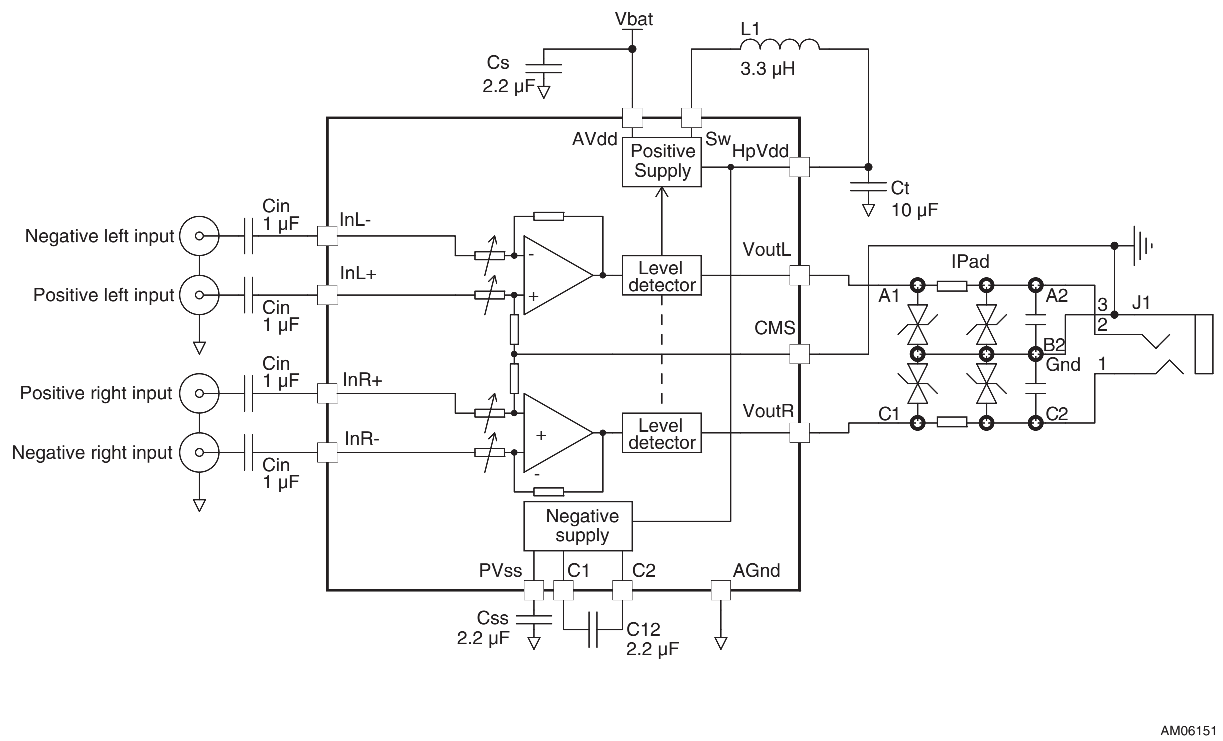
The A22H165 is designed to operate with a passive first-order low-pass filter (as shown in *Figure 1*). This low-pass filter is mandatory to ensure correct operation of the A22H165 over the volume range and output capacitance range vs. load.

R_{out} must have a value of 12 Ω minimum and C_{out} a value of 0.8 nF minimum up to 100 nF maximum. Values of 12 Ω and 1 nF are a good starting point for a design to be able to drive a classic headphone (16 Ω, 32 Ω, 60 Ω) and the line-in of any hi-fi system or sound card. The cutoff frequency of this filter (12 Ω and 1 nF) is approximately 13 MHz and clearly above the audio band.

However, this output RC filter is also a part of the IEC 61000-4-2 ESD protection. In most cases, this RC filter is designed with transient absorbers and the final solution can be a discrete solution or an integrated solution. ST Microelectronics' portfolio has many integrated solutions for ESD, but one dedicated to headphone amplifiers in particular: IPAD[a] reference EMIF02-AV01F3.

To fit the IEC 61000-4-2 standard, this audio line IPAD can be added to the output of the A22H165 as shown in *Figure 67*.

Figure 67. Typical application schematic with IEC 61000-4-2 ESD protection



By adding this ESD protection, the A22H165 complies with the IEC 61000-4-2 level 4 standard on jack pins. Our demonstration board has been tested using the same conditions

a. Copyright STMicroelectronics.

as those outlined in the IEC 61000-4-2 standard. Results may differ depending on the layout of the PCB.

- 15 kV (air discharge)
- 8 kV (contact discharge)

This IPAD has an internal series resistor R_{out} = 15 Ω +/-20 % and an output capacitor C_{out} = 3.2 nF +/-25 %.

4.3.7 Integrated input low-pass filter

The A22H165 has an integrated internal first-order low-pass filter with a -3 dB cutoff. This integrated filter is present on each input and filters any out-of-band audio noise coming from the audio source.

4.4 Single-ended input configuration

The A22H165 can be used in a single-ended input configuration. InR- and InL- or InR+ and InL+ can be shorted to ground through input capacitors. All C_{in} capacitors must have the same value to keep the same PSRR performance as in a differential input configuration. *Figure 68* and *Figure 69* show how to connect the A22H165. Note the ground connection of each input. To avoid PSRR issues resulting from any ground noise, this connection must be done on the ground of the audio source and not on the ground of the A22H165 itself.

Figure 68. Single-ended input configuration1

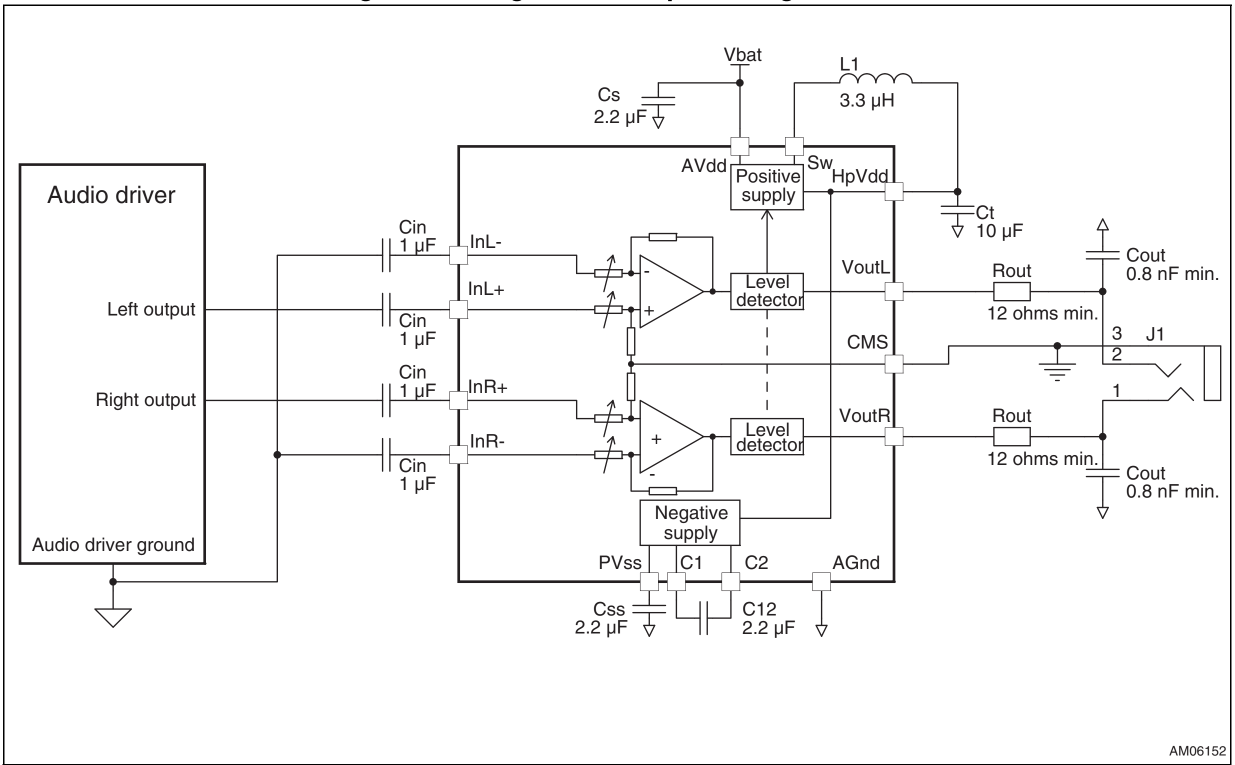
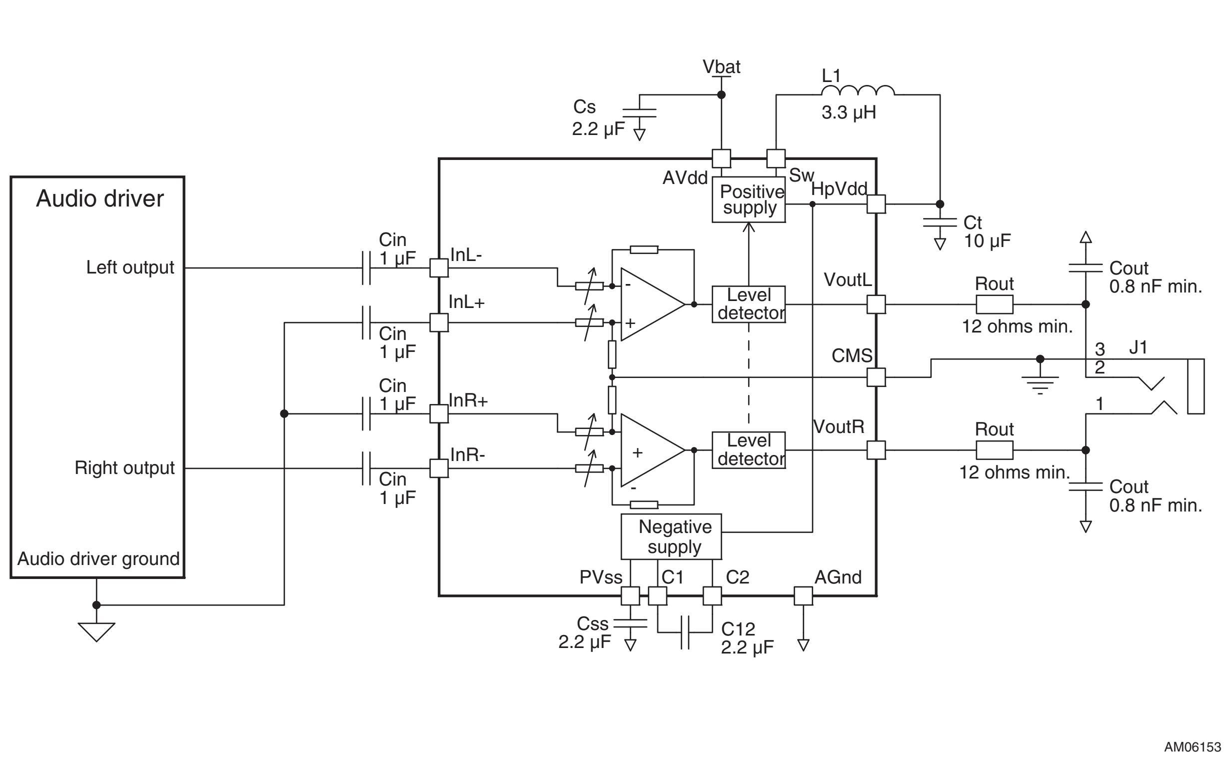


Figure 69. Single-ended input configuration 2



The gain range in these configurations remains unchanged and is given by:

$$VoutLR = VinLR \times Gain$$

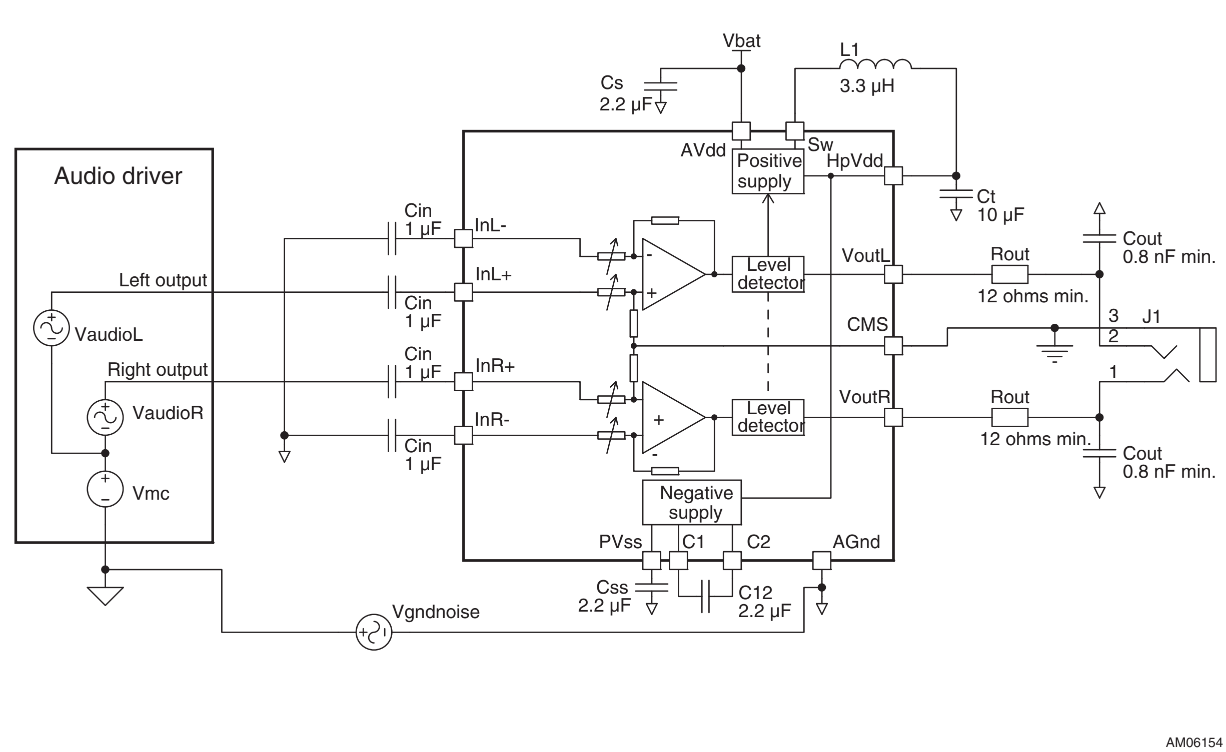
With reference to *Figure 69*, note that the absolute phase in the audio band is 180°.

4.4.1 Layout recommendations for single-ended operation

The connection location of each input that has to be set to ground is extremely important.

Incorrect connection location

Figure 70. Incorrect ground connection for single-ended option



If these inputs are connected to AGnd (the ground of the A22H165 class-G), the output voltage can be expressed by the following simplified equation from an AC point of view.

Equation 1

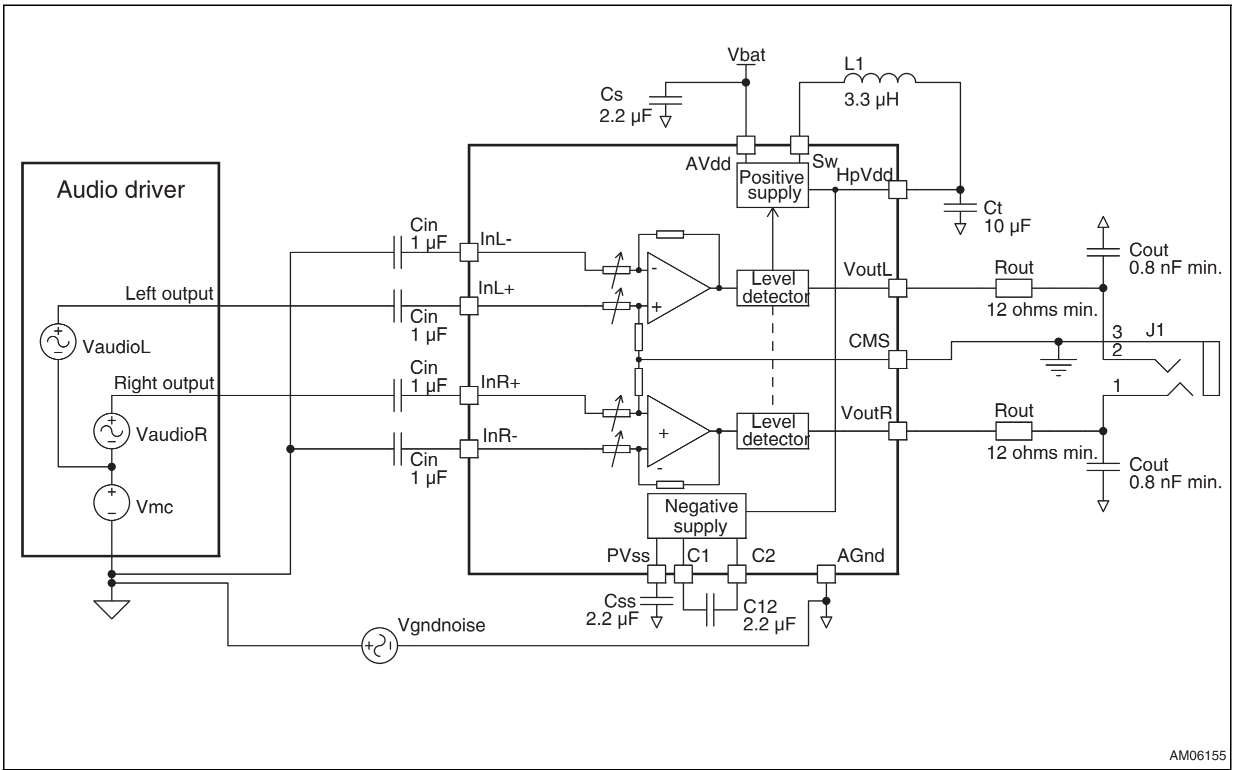
$$V_{out} = Av \times (V_{audio} + V_{mc} + V_{gndnoise}) + V_{batnoise} \times PSRR$$

As shown in *Equation 1*, any ground noise and any parasitic AC voltage on V_{mc} is directly multiplied by the gain of the amplifier. If V_{mc} can be totally controlled by the design of the audio source device (no parasitic AC voltage), it is not necessarily the case for $V_{gndnoise}$. This noise can be significantly reduced by an adequate low impedance ground plane, but not totally eliminated. In practice, only ten millivolts in the right frequency range are enough to produce an audible parasitic sound in the headphone with a volume level as low as -20 dB.

Correct connection location

As shown in *Figure 71*, the best option is to route the single-ended signal in parallel with the AC ground line of the other input. The AC grounded terminal must be routed in parallel to the audio signal and grounded with the ground of the audio source.

Figure 71. Correct ground connection for single-ended option



In this configuration, the AC output voltage is:

Equation 2

V_{out} = Av x (Vaudio + Vmc) + Vgndnoise x CMRR + Vbatnoise x PSRR

In *Equation 2* the ground noise is attenuated by the performance of the CMRR. In practice, 50 dB of CMRR and ten millivolts for ground noise gives an output of approximately 30 µV, which is normally too low to be perceptible in the headphone. If V_{mc} is also totally controlled by the design of the audio source, *Equation 2* becomes:

Equation 3

V_{out} = Av x Vaudio + Vbatnoise x PSRR

Like in differential mode, the main contributor for audio signal degradation is the AC noise voltage on V_{bat}. Thanks to the A22H165's very high PSRR that can attenuate GSM burst noise, *Equation 3* becomes:

Equation 4

V_{out} = Av x Vaudio

4.5 Startup phase

The A22H165 uses different techniques to reduce the DC current consumption and offer a pop-and-click performance close to none.

4.5.1 Auto zero technology

During the startup phase, the differential output voltage is sensed and adjusted to 0 V (+/-500 µV) to avoid any pop noise when the amplifier becomes operational. This also helps to minimize extra current consumption due to the load (Icc-extra = VoutDC / Rload).

4.5.2 Input impedance

The A22H165 requires input coupling capacitors. The usual lowest frequency used for the headphone is close to 20 Hz. This frequency means a constant time for a first-order high-pass filter of approximately 1 / (2 x Pi x 20) = 8 ms.

To achieve 95 % of the capacitor’s charge, it is necessary to wait 3 x 8 ms = 24 ms, which is out of range for a device with a fast startup time.

Because of the mismatching of all input capacitors and input resistors, if it is decided to start the A22H165 at a time of 8 ms, a voltage difference at the inputs (multiplied by the gain) can create a voltage step on the output and consequently a pop noise.

To avoid this issue during the starting phase, the A22H165 accelerates the charging of the input capacitors by reducing the input impedance to 2 kΩ.

In such a case, for a 1 µF capacitor the 95 % charge is reached in 6 ms. As the startup time of A22H165 is 12 ms, there remains sufficient time to fully charge the input capacitors and as such eliminate any pop noise.

4.6 Layout recommendations

Particular attention must be given to the correct layout of the PCB traces and wires between the amplifier, load and power supply (in most cases, the battery of the cellular phone).

The power and ground traces are critical since they must provide adequate energy and grounding for all circuits. Good practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

A track with a width of at least 200 µm for a copper thickness of 18 µm is recommended for bringing energy to the amplifier from the battery.

Proper grounding guidelines help improve audio performances, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. It is also recommended to use a large-area and multi-via ground plane to minimize parasitic impedance.

A multi-layer PCB board allows double or multiple ground planes to be implemented. Most of the time, the top and bottom layers are used as ground planes and provide shielding for tracks routed on the intermediate layers. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

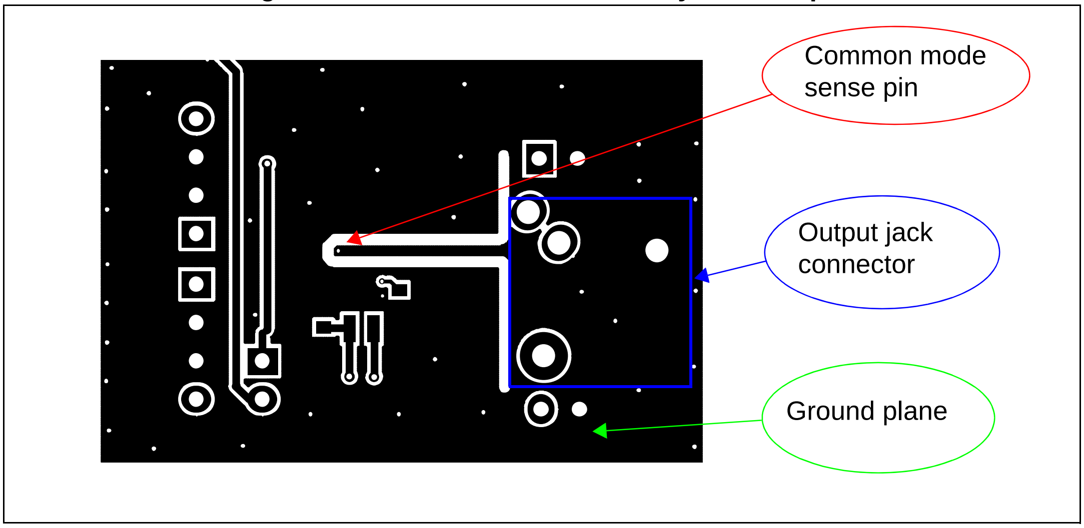
The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize the trace resistances.

4.6.1 Common-mode sense layout

The A22H165 implements a common-mode sense pin to correct any voltage differences that might occur between the return of the headphone jack and the AGND of the device that can create parasitic noise in the headphone and/or line out.

The solution to strongly reduce and practically eliminate this noise consists in connecting the headphone jack ground to the CMS pin. This pin senses the difference of potential (voltage noise) between the A22H165 ground and the headphone ground. Thanks to the frequency response and the attenuation of the common-mode sense pin, this noise is removed from the A22H165 outputs.

Figure 72. Common-mode sense layout example



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 73. A22H165 footprint recommendation

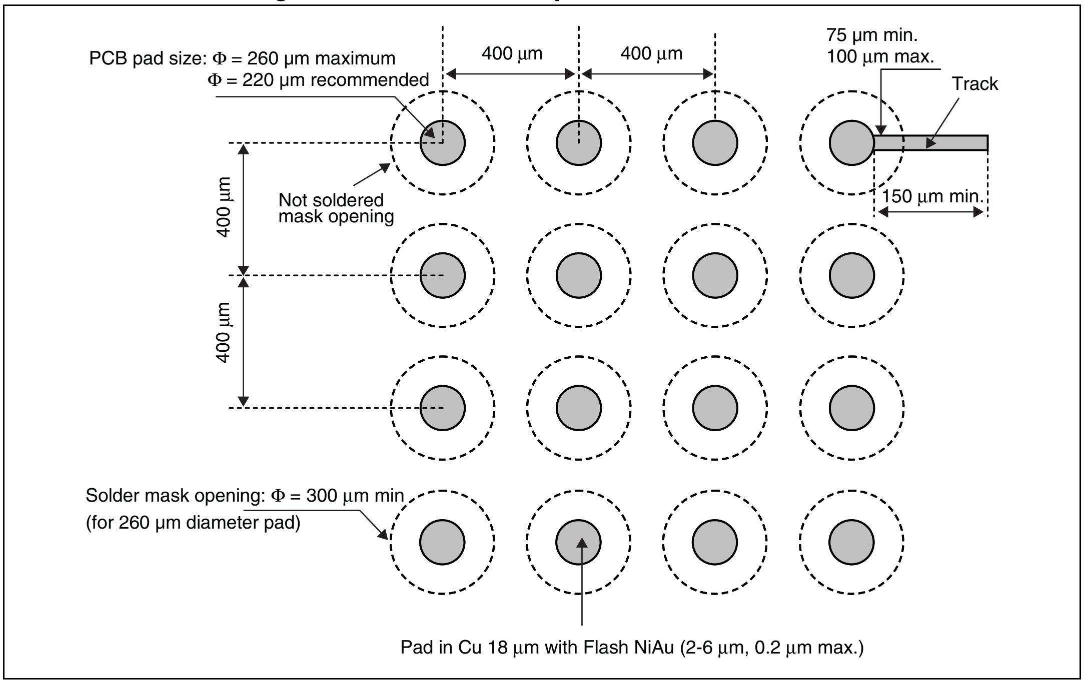


Figure 74. Pinout

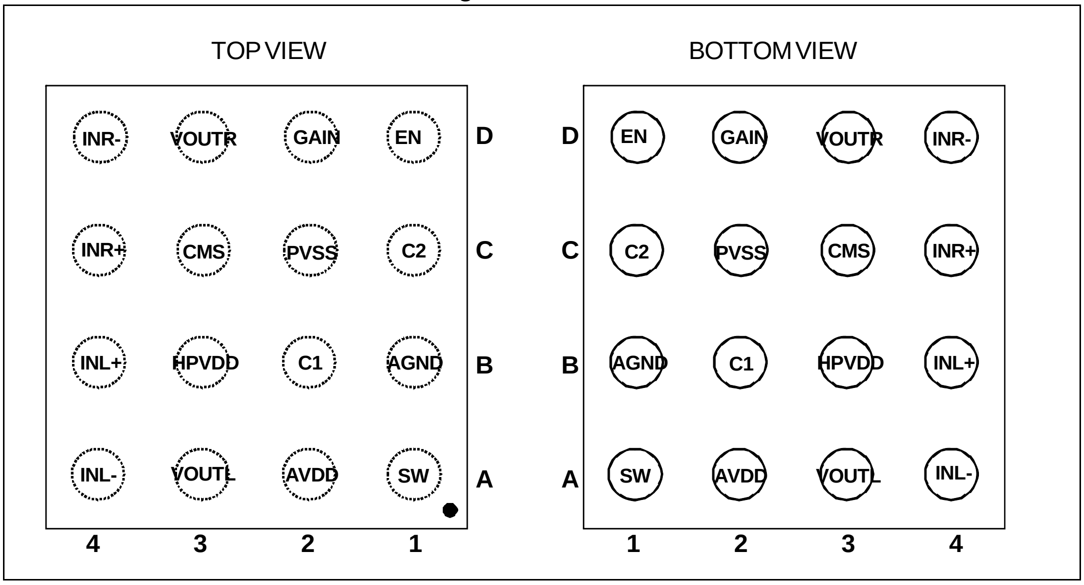


Figure 75. Marking (top view)

- Logo: ST
- Symbol for lead-free: E
- Part number: 21
- X digit: Assembly code
- Date code: YWW
- The dot marks pin A1

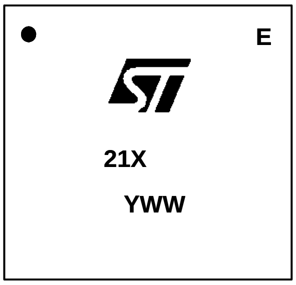
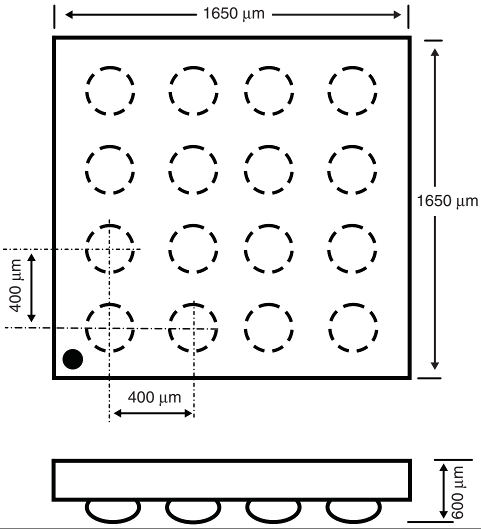
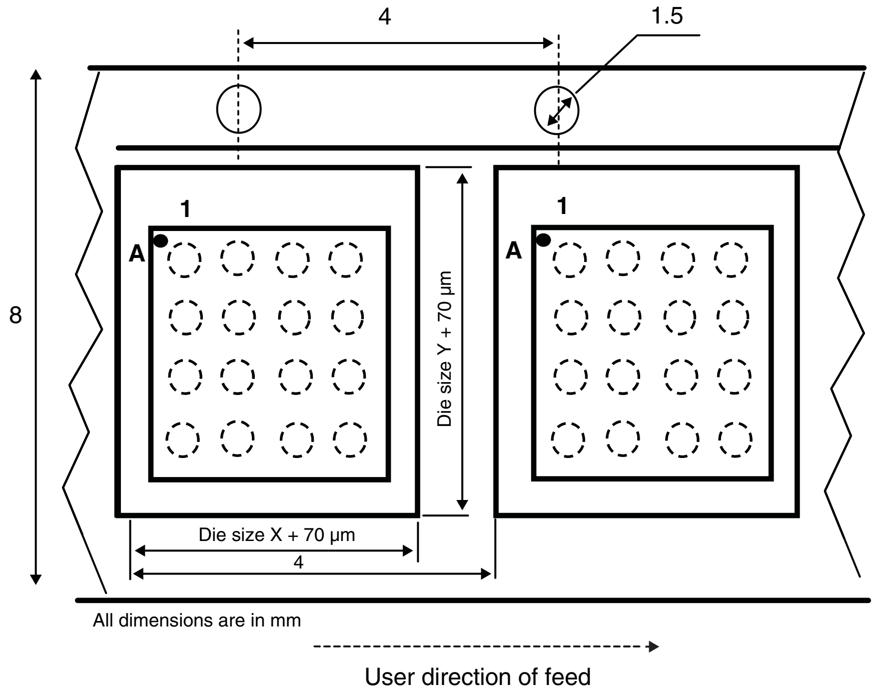


Figure 76. Flip-chip - 16 bumps



- Die size: 1.65 mm x 1.65 mm ± 30 µm
- Die height (including bumps): 600 µm ±55 µm
- Bump diameter: 250 µm ±40 µm
- Bump height: 205 µm ±35 µm
- Die height: 395 µm ±20 µm
- Pitch: 400 µm ±40 µm
- Coplanarity: 50 µm max

Figure 77. Device orientation in tape pocket



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
06-Mar-2014	1	Initial release.