

	REVISIONS															
	LTR	DESCRIPTION						DATE				APPROVED				
	A	Change to the B1 dimension in figure 2. Add pulse application paragraph. Editorial changes throughout.						12 NOV 2009				M. Radecki				
Prepared in accordance with ASME Y14.100 Source control drawing																
REV STATUS OF PAGES	REV	A	A	A	A	A	A									
	PAGES	1	2	3	4	5	6									
PMIC N/A	PREPARED BY Andrew R. Ernst						DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OH									
Original date of drawing 17 November 2006	CHECKED BY Andrew R. Ernst						TITLE RESISTOR, CHIP, FIXED, FILM, 8 PIN ARRAY, STYLE 1206									
	APPROVED BY Michael Radecki															
	SIZE A	CODE IDENT. NO. 037Z3					DWG NO. 07005									
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1. SCOPE

1.1 Scope. This drawing describes the requirements for a multi resistive function in a single chip package.

1.2 Part or Identifying Number (PIN). The complete PIN is as follows:

07005	X	XXXX	X	X	X	X	X
Drawing number	Characteristic (see 3.3.1)	Resistance (see 3.3.2)	Tolerance (see 3.3.3)	Schematic (see 3.3.4)	Termination (see 3.3.5)	Screening level (see 3.3.7)	Configuration (see 3.3.8)

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-55342 - Resistor, Chip, Fixed, Film, Nonestablished Reliability, Established Reliability, Space Level, General Specification for.

* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.2 Order of precedence. Unless otherwise noted herein or in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with **MIL-PRF-55342** and as specified herein.

3.2 Interface, and physical dimensions. The resistor shall meet the interface, and physical dimensions as specified in **MIL-PRF-55342** and herein (see [figure 2](#)).

3.3 Electrical characteristics.

3.3.1 Resistance temperature characteristic. The resistance temperature characteristic shall be available in characteristics K (± 100 ppm), L (± 200 ppm) and M (± 300 ppm).

3.3.2 Resistance. The nominal resistance expressed in ohms is identified by four digits; the first three digits represent significant figures and the last digit specifies the number of zeros to follow. When the value of resistance is less than 1,000 ohms, or when fractional values of an ohm are required, the "R" shall be substituted for one of the significant figures. The resistance value designations are shown in [table I](#). Appropriate values not listed in the "10 to 100" decade table of **MIL-PRF-55342** for the appropriate resistance tolerance shall be considered as not conforming to the specification.

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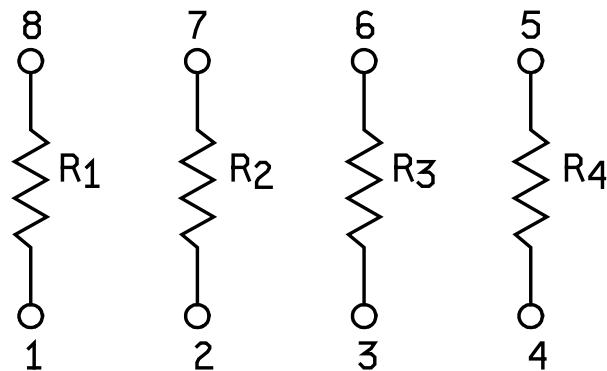
TABLE I. Resistance value designations.

Designation	Resistance ohms			
10R0 to 97R6 inclusive	10.0	to	97.6	inclusive
1000 to 9760 inclusive	100	to	976	inclusive
1001 to 9761 inclusive	1,000	to	9,760	inclusive
1002 to 9762 inclusive	10,000	to	97,600	inclusive
1003 to 9763 inclusive	100,000	to	976,000	inclusive
1004	1,000,000			

3.3.2.1 Resistance range. The resistance range shall be 10 ohms to 1.0 megohms.

3.3.3 Resistance tolerance. The resistance tolerance shall be available in F (± 1 percent), G (± 2 percent), and J (± 5 percent) tolerance.

3.3.4 Schematic. The schematic of the chip array shall be identified by a single letter in accordance with [figure 1](#).



SCHEMATIC A

FIGURE 1. Schematic chip resistor array.

3.3.5 Termination. Termination shall be in accordance with [MIL-PRF-55342](#).

3.3.6 Pure tin. The use of pure tin, as an underplate or final finish is prohibited both internally and externally. Tin content of resistor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see [6.3](#)).

3.3.7 Screening level. The screening level shall consist of five levels; Level A shall be the thermal shock of [MIL-PRF-55342](#), group A, subgroup 2 followed by the short time overload described in [3.3.7.1](#), followed by the dc resistance test of [MIL-PRF-55342](#). Level B shall be only the short time overload test as described in [3.3.7.1](#), followed by the dc resistance of [MIL-PRF-55342](#). Level C shall be the non-ER (C level) test as described in [MIL-PRF-55342](#). Level D shall be the ER test as described in [MIL-PRF-55342](#). Level E shall be the space level test as described in [MIL-PRF-55342](#).

3.3.7.1 Short time overload. The short time overload test shall consist of 2.5 times rated voltage for 5 seconds at room temperature, not to exceed twice the maximum continuous working voltage.

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- 3.3.8 Configuration. Configuration A shall be in accordance with [figure 2](#).
- 3.3.9 Power rating. The power rating for schematic A shall be as specified in [table II](#).

TABLE II. Power rating

Schematics	Characteristics K, L and M	
	Element (watts)	Network (watts)
A	0.050	0.250

- 3.3.10 Voltage rating. The maximum continuous working voltage shall not exceed 50 volts dc.

- 3.4 Marking. Marking is not required on the resistor; however each unit package shall be marked with the PIN assigned (see [1.2](#)), manufacturer's identification code, and date and lot codes.
- 3.5 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.
- * 3.6 Manufacturer eligibility. To be eligible for listing as a approved source of supply, a manufacturer shall be listed on the [MIL-PRF-55342](#) Qualified Products List for at least one part, or perform the group A and group B inspections specified herein on a sample agreed upon by the manufacturer and DSCC-VA.
- * 3.6.1 Certificate of compliance. A certificate of compliance shall be required from manufacturers requesting to be listed as an approved source of supply.

- 3.7 Workmanship. Resistors shall be uniform in quality and free from defects that will affect life, serviceability, or appearance.

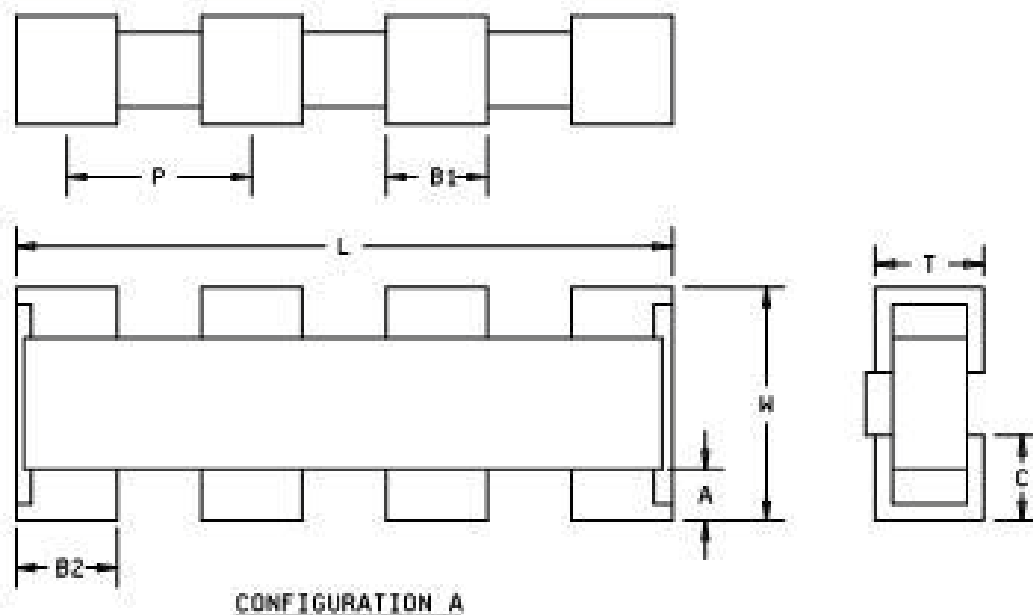
4. VERIFICATION

- 4.1 Qualification inspection. Qualification inspection is not applicable to this document.
- 4.2 Conformance inspection.
 - 4.2.1 Inspection of product for delivery. Inspection of product for delivery for levels A and B shall consist of subgroups 1, 2, and 3 (as modified in [3.3.7](#)) of group A and group B inspection of [MIL-PRF-55342](#). Levels C, D, E shall consist of group A and group B inspection of [MIL-PRF-55342](#).
 - 4.2.2 Mounting integrity. Mounting integrity shall be performed in accordance with [MIL-PRF-55342](#), except the applied force shall be 2Kg.
 - 4.2.3 Certification. The procuring activity may accept a certificate of compliance in lieu of group B inspection (see [6.2d](#)).

5. PACKAGING

- 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see [6.2](#)). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

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Configuration	A	B1	B2	C	L	P	T	W
A	0.010 (0.254)	0.018 (0.457)	0.025 (0.635)	0.015 (0.381)	0.125 (3.175)	0.030 (0.762)	0.020 (0.508)	0.063 (1.600)

NOTES:

1. Dimensions are in inches.
2. Metric equivalents in parenthesis are given for general information only.
3. Unless otherwise specified, tolerances are ± 0.005 inches (0.13 mm).
4. The picturization of the resistor above is a given representative of the envelope of the item. Slight deviations from the outline shown, which are contained within the envelope, and do not alter the functional aspects of the device are acceptable.
5. As a minimum the coating shall cover the total element of the resistor.

FIGURE 2. Chip resistor array.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Chip resistor arrays are intended for use in thick or thin film circuits where microcircuitry is intended. Chip resistor arrays can also be used in surface mount applications.

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6.2 Ordering data. The contract or purchase order should specify the following:

- a. Complete PIN (see 1.2).
- b. Requirements for delivery: One copy of the conformance inspection data or certification of compliance that parts have passed conformance inspection with each shipment of parts by the manufacturer.
- c. Requirements for packaging and packing.
- d. Whether the manufacturer performs the group B inspection or provides a certificate of compliance (see 4.2.3).

6.3 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to [ASTM-B545](#) (Standard Specification for Electrodeposited Coatings of Tin).

6.4 Electrostatic charge. Under several combinations of conditions, these resistors can be electrically damaged, by electrostatic charges, and drift from specified value. Users should consider this phenomena when ordering or shipping resistors. Direct shipment to the Government is controlled by [MIL-DTL-39032](#) which specifies a preventive packaging procedure.

* 6.5 Pulse applications. Designers are CAUTIONED on using the above resistors in high power pulse applications. Since they have not been qualified nor tested for such applications, damage and premature failure are possible. These resistors only see a one time pulse (Short-time overload) as part of the group B inspection of [MIL-PRF-55342](#).

* 6.6 User of record. Coordination of this document for future revisions is coordinated only with the approved source of supply and the users of record of this document. Requests to be added as a recorded user of this drawing may be achieved online at resistor@dla.mil or in writing to: DSCC-VAT, Post Office Box 3990, Columbus, OH 43218-3990 or by telephone (614) 692-0552 or DSN 850-0552.

* 6.7 Approved source of supply. Approved source of supply is listed herein. Additional sources will be added as they become available. Assistance in the use of this drawing may be obtained online at resistor@dla.mil or contact DSCC-VAT, Post Office Box 3990, Columbus, OH 43218-3990 or by telephone (614) 692-0552 or DSN 850-0552.

DSCC drawing PIN 07005	Vendors similar Designation or type Number 1/	Vendor CAGE	Vendor's name and address
Characteristics; K, L, M Resistance: 10 ohms to 1 megohms; Tolerance: 1, 2, 5 percent; Schematic A; All terminations; Screening levels: C, D, E; Configuration: A	HD0608***** (D07005)	56235	State of the Art, Inc. 2470 Fox Hill Road State College, PA 16803-1797

1/ Parts must be purchased to the DSCC PIN to assure that all performance requirements and tests are met.

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